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Comparison of Multilevel Inverter Topologies Using MATLAB/SIMULINK

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ABSTRACT: In the multilevel inverter sine wave can be approximated to a stepped waveform having large number of steps. As the number of levels in the inverter increases the harmonic distortion at the inverter output decreases. The diode clamped inverter and the H bridge inverter topologies for the multilevel inverters have been discussed along with their simulations. In this paper, a new multi-level inverter topology has been proposed to further reduce the harmonic distortion in the multi-level inverters. It's simulation and the output results have been discussed. Also, a comparison of all the multi-level inverters has been done.

Keywords: *Cascaded H bridge Inverter, Diode Clamped Inverter, Multilevel Inverter Topology, Sine Pulse Width Modulation (SPWM), Total Harmonic Distortion (THD)*

I. INTRODUCTION

An inverter is an electronic circuitry that converts the direct current into alternating current. The two level inverters have to switch between the two extreme levels of the dc-link voltages and hence the rate of voltage (dv/dt) is very high in every switching. This (dv/dt) causes additional EMI and increases the stress on machine winding insulation. The distortion is also high in case of two level inverters. Thus due to the above mentioned limitations use of conventional two-level inverters employing PWM techniques is restricted to low and medium power applications. As multi-level inverters are capable of generating output voltages with very low distortion and dv/dt, generating smaller common-mode voltage and operating with lower switching frequency as compared to the two-level inverters, they are highly in demand. Multi-level inverters generate output voltage with stepped waveforms by using an array of power semiconductors and capacitor voltage sources. Multi-level inverters offer various advantages as compared to the two-level inverters, of which some are as follows:

- They reduce the *total harmonic distortion* (THD) in voltage by increasing the number of steps.
- They can be operated at lower frequencies, thus reducing the switching losses.
- By reducing the switching dv/dt, the EMI problems can be reduced.
- They allow the use of power semiconductor devices of low ratings to realise high voltage levels at the inverter output.

Multi-level inverters are extensively used in high-power drive applications for laminators, mills, conveyors, pumps, fans, blowers, compressors, etc.

II. MULTILEVEL INVERTER TOPOLOGIES

A. Diode Clamp Inverter

As shown in fig.1 diode clamped inverter needs only one DC-bus and the voltage levels are produced by several capacitors in series. If the inverter is so designed that each blocking diode has the same voltage rating as the active switches, n blocking diodes will be required in series; consequently, the number of diodes required for each phase would be (m-1) × (m-2). Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter.

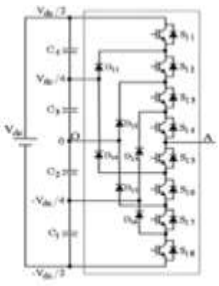

Fig.1: One leg of 3-level diode clamped inverter topology

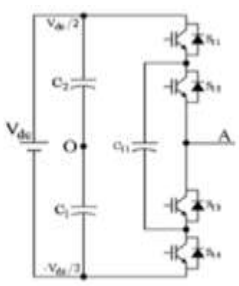

Fig.2: One leg of a flying capacitor inverter topology

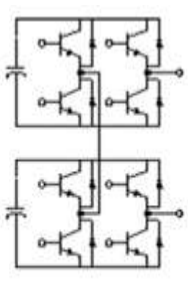

Fig.3: One leg of a cascaded H-bridge inverter topology

B. Flying Capacitor Inverter

One leg of a flying capacitor inverter topology is shown in fig.2. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The m-level flying-capacitor multi-level inverter requires (m-1) dc-link capacitors and (m-1) × (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches.

C. Cascaded H-Bridge Inverter

One leg of a cascaded H-bridge inverter topology is shown in fig.3. The cascaded inverter needs isolated DC supplies for each DC-bus. This causes the DC-bus structure to be very complicated. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources.

The simulation for all the inverter topologies has been carried out using the SPWM technique. In the PWM technique the reference or the modulating signal is compared with the carrier signal to generate the output. The number of carrier signals to be used depend on the level of the inverter. The modulating signal used is a sine wave, irrespective of the level of the inverter. For an *n* level inverter, the number of carrier signals to be used will be *(n-1).*

III. DIODE CLAMP INVERTER

A. Three Level And Five Level Inverters

Simulation of the three level and five level diode clamp bridge inverters is carried out using the sine pulse width modulation technique with help of MATLAB/SIMULINK. Simulation was carried out to observe the line voltage THD for R load. For a three level inverter the modulating signal, i.e sine wave is compared with two carrier signals, i.e triangular wave. For a five level inverter the modulating signal, i.e sine wave is compared with four carrier signals, i.e triangular waves. The output of the inverter and the THD analysis are as shown below.

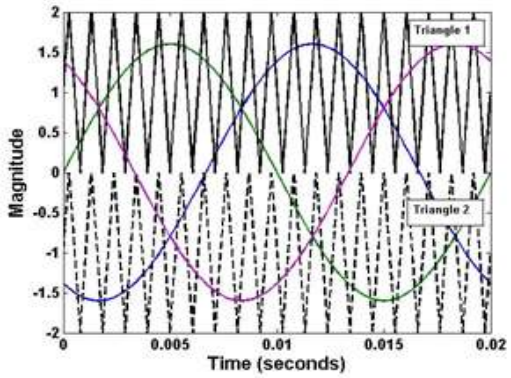

Fig.4: Gate pulse to the switches of 3 level diode clamped inverter

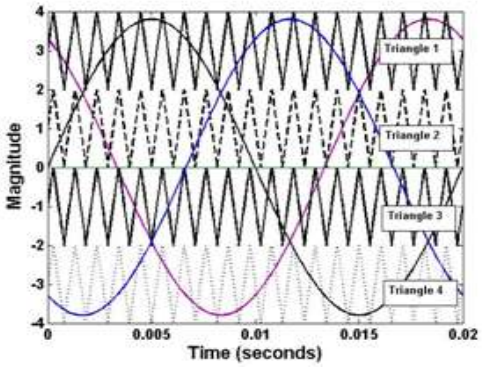

Fig.5: Gate pulse to the switches of 5 level diode clamped inverter

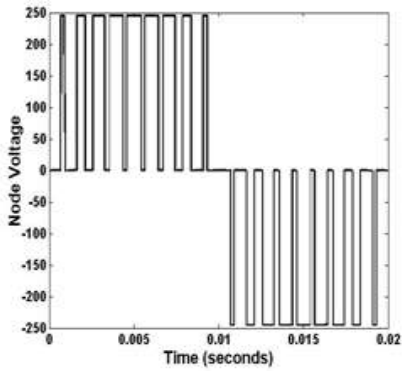

Fig.6: Node voltage of the 3 level diode inverter

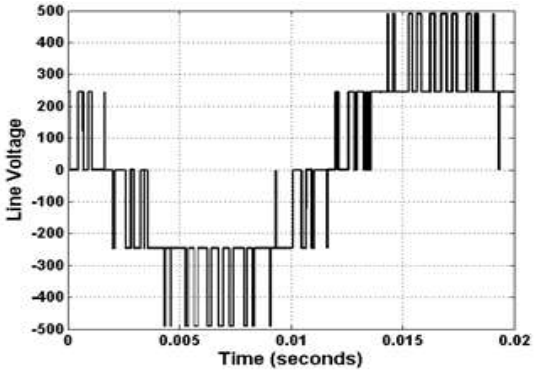

Fig.7: Line voltage of the 3 level diode clamped clamped inverter

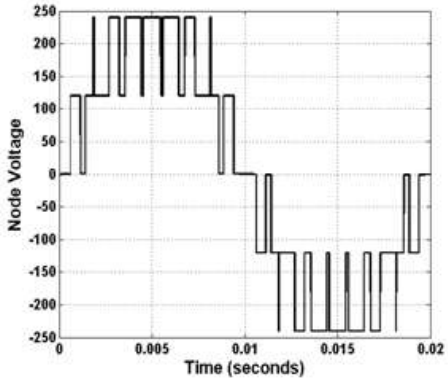

Fig.8: Node voltage of the 5 level diode clamped inverter

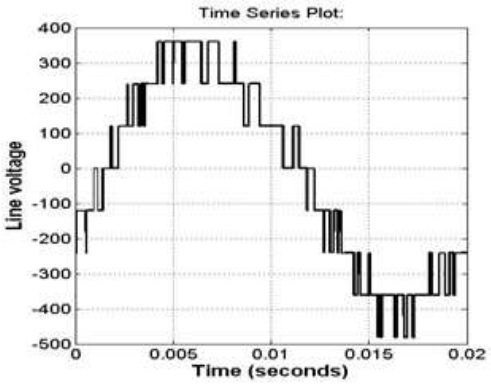

Fig.9: Line voltage of the 5 level diode clamped inverter

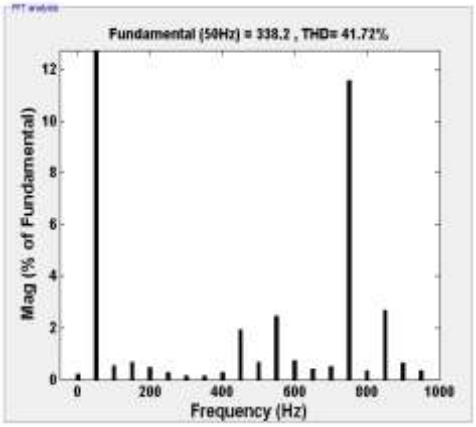

Fig.10: THD analysis of a 3 level diode clamped inverter

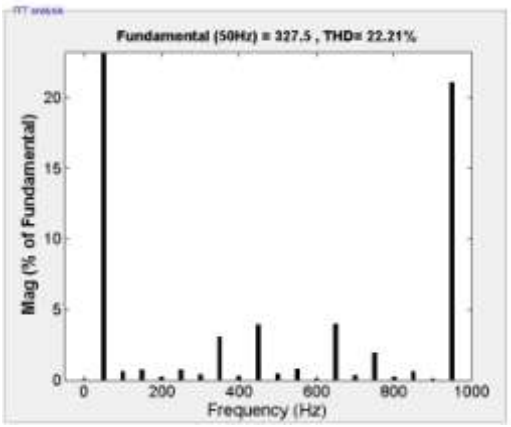

Fig.11: THD analysis of a 5 level diode clamped inverter

IV. H-BRIDGE INVERTER

A. Three Level And Five Level Inverters

Simulation of the three level and five level H-bridge inverters is carried out using the sine pulse width modulation technique with help of MATLAB/SIMULINK. Simulation was carried out to observe the line voltage THD for R load. For a three level inverter the modulating signal, i.e sine wave is compared with two carrier signals, i.e triangular wave. For a five level inverter the modulating signal, i.e sine wave is compared with four carrier signals, i.e triangular waves. The output of the inverter and the THD analysis are as shown below.

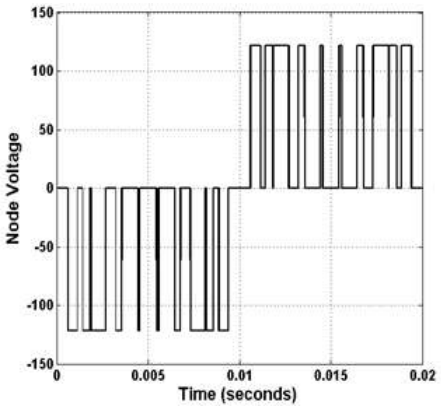

Fig.12: Node voltage of a 3 level H bridge inverter

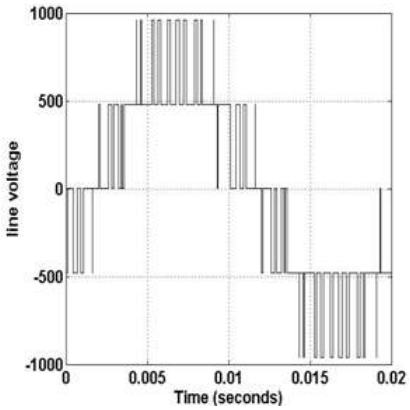

Fig.13: Line voltage of a 3 level H bridge inverter

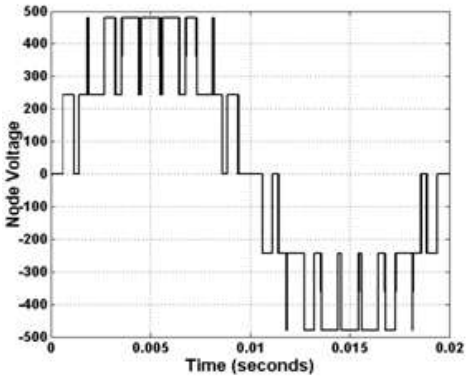

Fig.14: Node voltage of a 5 level H-bridge inverter

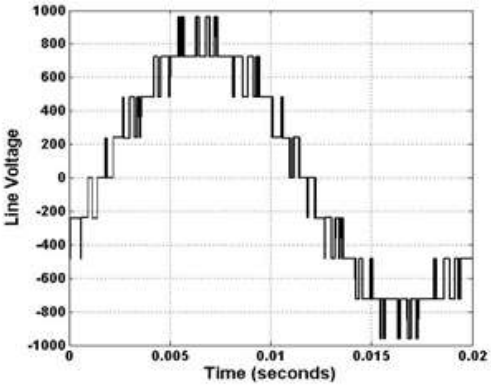

Fig.15: Line voltage of a 5 level H-bridge inverter

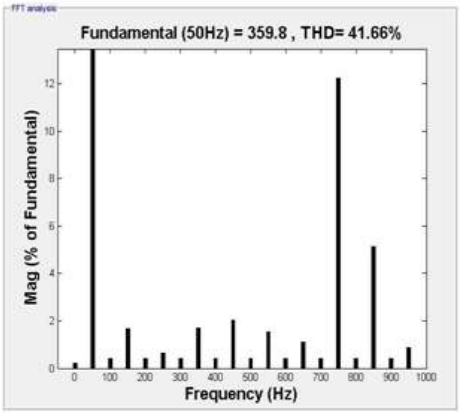

Fig.16: THD analysis of a 3 level H-bridge inverter

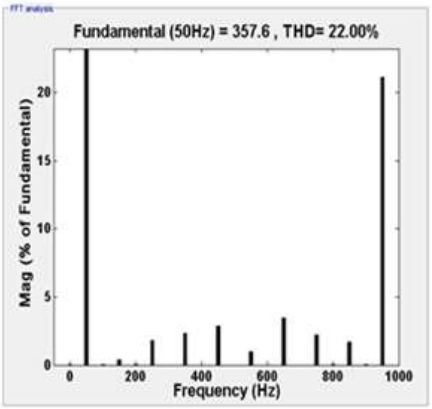

Fig.17: THD analysis of a 5 level H-bridge inverter

V. PROPOSED TOPOLOGY

Simulation of the proposed topology is carried out using the sine pulse width modulation technique with help of MATLAB/SIMULINK. Simulation was carried out to observe the THD of line voltage for R load.

At wt =0 by triggering the s6, s1 and s4 switches the output voltage is + Vdc/2. For + Vdc, the swiches s5 ,s1 and s4 are triggered. By triggering the s6,s2 and s3 switches the output voltage is - Vdc/2. For the -Vdc, the swiches s5 ,s2 and s3 are triggered. The simulation circuit, output of the inverter and the THD analysis are as shown in fig.18, fig.19 and fig.20 respectively.

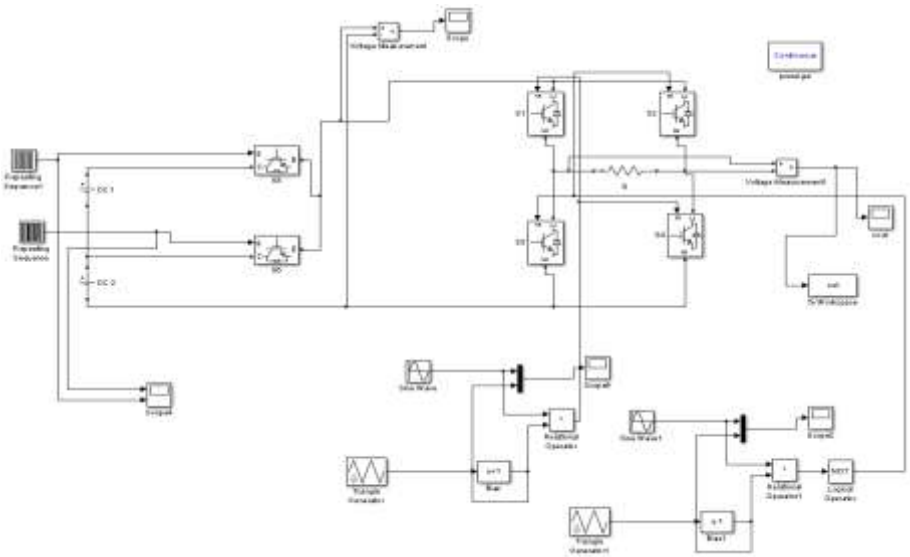

Fig.18: Simulation circuit of the inverter based on the proposed topology

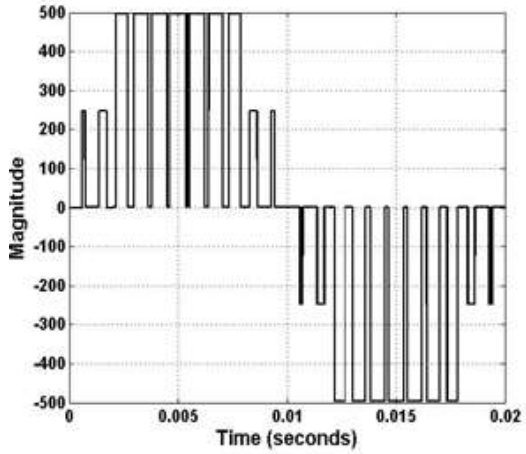

Fig.19: Output of thel inverter based on the proposed topology

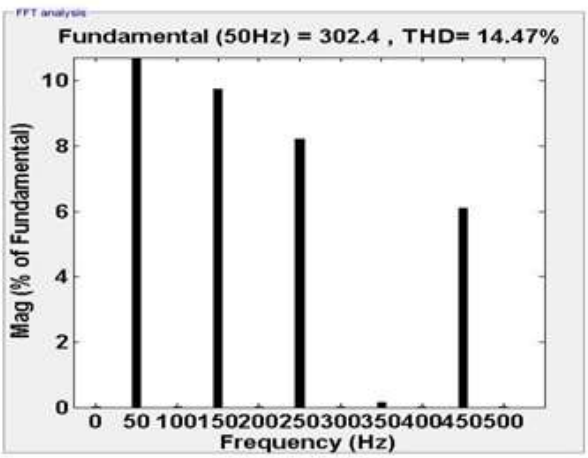

Fig.20: THD of the inverter based on the proposed topology

VI. COMPARISON

The comparison of all the inverter topologies has been done and the results have been compiled in the table below. The source voltage for all the inverter topologies has been kept constant at 500v. The modulation index, i.e the ratio of amplitude of modulating signal to the amplitude of carrier signal, has been kept constant at 0.8.

Table I: Comparison of all the inverter topologies

Inverter Topology	Level of Inverter	Number of DC Source	Number of Capacitors	Number of Switches	Number of Diodes	THD (%)
Diode Clamp	3	1	2	12	6	41.72
Diode Clamp	5	1	4	24	18	22.21
H-Bridge	3	6	6	24	0	41.66
H-Bridge	5	6	6	24	0	22.00
Proposed Topology	5	2	0	6	4	14.47

VII. CONCLUSIONS

The THD in two-level and multi-level inverters were compared. It was found that the two-level configuration has higher THD than the three-level configuration. The different three-level converter topologies were studied and the diode clamped inverter was found to be most beneficial because it uses only one DC-bus and produces the different voltage levels by capacitors in series. The proposed topology, however , was the most efficient of all. The proposed topology had only 14.47 % THD as compared to 22.21 % and 22 % in 5 level diode clamp bridge inverter topology and 5 level H bridge topology respectively. Further the components used in the proposed topology such as capacitors, diodes and switches were less in number then the diode clamp inverter and H bridge inverter topologies.

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