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Novel Low Power Hybrid Adders Using 90nm Technology for DSP Applications

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Abstract—In this paper, two novel Hybrid Adders are proposed for Multiplier Accumulator Unit (MAC) of low power DSP application. Adders are the most important component of the MAC unit which can significantly affect the efficiency of the whole system. Thus, power reduction in Full adder circuit is essential for low power applications. These novel full adders are simulated in 90 nm Technology with BSIM model at 27° temperature. The performance of power, delay, voltage swing, power delay product and area of these Hybrid adders are studied at various low supply voltages (0.8V, 0.9V & 1.0V), and compared with the other five adders. The Hybrid- A full adder which shows better delay performance than the other adders and Hybrid –B full adder which shows lower power consumption, operates at low voltage with good signal integrity, thereby making them suitable for low power high performance applications.

Keywords— Low power; MAC unit; full adder; dynamic power; Power Delay Product.

I. INTRODUCTION

Due to the rapid growth in portable electronics and communication systems like laptops, etc., the low power microelectronic devices have become very important in today's world [1]. In fact, Low-power VLSI chips have emerged in high demand for designing any sub system. With the increase in complexity of VLSI systems and amount of power available in certain systems like cell phones and digital cameras, minimizing power consumption is essential. Further, lower power consumption in system is essential for many applications due to the dramatic increase in power-conscious applications. These low power circuits can be realized using both hardware and software approach. In many VLSI applications, arithmetic operations are used extensively. Mostly the digital processing requires high speed and low power multiplier accumulator (MAC) unit. Addition and multiplication are the most important operations in this unit. Specifically, speed and power efficient implementation of these adders is a very challenging problem. Lowering power consumption not only increases reliability, but also saves package costs due to reduced heat dissipation. The main contributor to overall power dissipation in CMOS VLSI circuits is dynamic power consumption which accounts for up to 80% of the total power [1-2]. The dominant source of power dissipation is the dynamic power dissipation due to the charging and discharging of the node capacitances and is given by:

$$P=0.5\, CV_{dd}^{2}\, E\,(sw)\, f_{clk} \qquad (1)$$

Where C is the physical capacitance of the circuit, V_{dd} is the supply voltage, E(sw) (switching activity) is the average number of transitions in the circuit per $1/f_{clk}$ time, and f_{clk} is the clock frequency. In order to reduce the power consumption of the adders any one of the above factors of circuit needs to be changed. In this work different logic structures are used for constructing adders for the low power DSP application.

This paper is organized as follows: the full adder cell for MAC unit is described in the section II, associated work for full adders is described in the section III, proposed two new Hybrid adders are given in section IV, simulation results and discussion is presented in the section V and finally conclusion is given in the section VI.

II. FULL ADDER CELL

Generally, a full adder is defined as a logical cell that performs an addition operation on three one-bit binary numbers. The full adder produces a two-bit output which is Carry and Sum. Full Adder cell is implemented in low power and high performance data path circuits of any system. The full adder consists of three input signals, i.e., A, B, and C (carry in), and two output signals Sum and Carryout which is shown in Fig. 1.

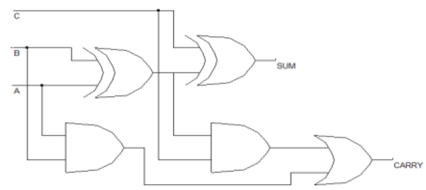


Fig.1. Full Adder cell

The basic operation of full adder is given by the standard Boolean expressions as,

$$C = AB + BC + CA \tag{2}$$

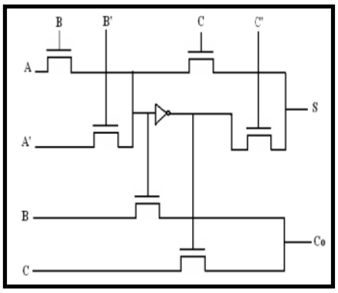
$$S = ABC + A'B'C + AB'C' + A'BC' \tag{3}$$

There are various design techniques for implementation of full adder circuits. Some of them are Multiplexing Control Input Technique (MCIT), Gate Diffusion Input technique (GDI), Technique based on static CMOS Inverter, Multi-threshold CMOS circuit technique (MTCMOS) [4-13]. The existing Shannon based full-adder cell has been executed for the sum operation and the carry operation separately. This has the demerits of more number of transistors, higher power consumption, larger area requirement, and pass transistor logic threshold voltage loss problem. In order to overcome the drawback of existing full adder circuits, the proposed full adder circuits has been implemented with different logic style and logic function. In the proposed full adder cell, Pass transistor logic is utilized among all the other logic styles available as it is found to enhance the circuit performance in terms of speed, power and transistor counts. The adder cell can be applied to implement low power and high performance data path circuits.

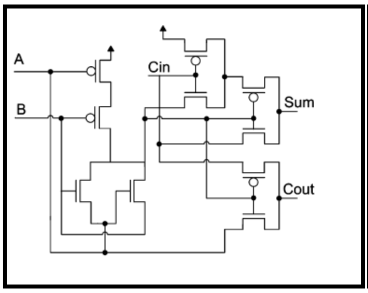
In this paper, different full adder circuits Modified Shannon, , Full adder using 10T, Full adder using 14T , Full adder using 16T, Hybrid FA-I [8-9] are simulated and analyzed the performance using the software tool HSPICE with 90nm technology. Two New Novel Hybrid FAs are proposed and its performances are studied. The main attributes are High-speed and high-resolution, ultra low power consumption, robust performance, immunity to noise & manufacturing variations.

III. RELATED WORK

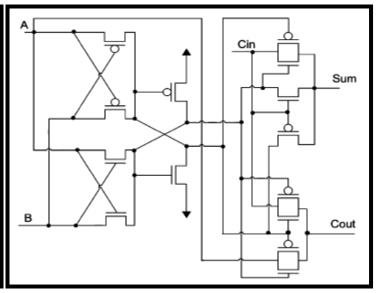
Adders are the basic building module in all multipliers, filters and MAC unit of DSP processor. So employing fast adders plays a key role in the performance of the entire all data path circuits. In this section different adder cells are described and analyzed. By using Shannon's theorem the sum and the carry expressions are condensed and thereby the transistor count has been decreased [7]. In the existing design of full adder the carry is generated using six transistors where as the modified Shannon full Adder [10] design uses only two transistors. Thus the total chip area gets reduced. Therefore the power has also been minimized to a considerable amount. (Fig .2.a). The advantage of the Modified shannon is lower number of transistors, and better voltage swing. Full adder using 10T use more than one logic structure for the implementation and is called as mixed logic design structure [11]. The numbers of transistors required to implement this circuit is 10 and A, B and Cin are the inputs. Sum and Carry are the outputs (see Fig. 2 .b). The demerits of this circuit are that produces high capacitance values for the inputs.



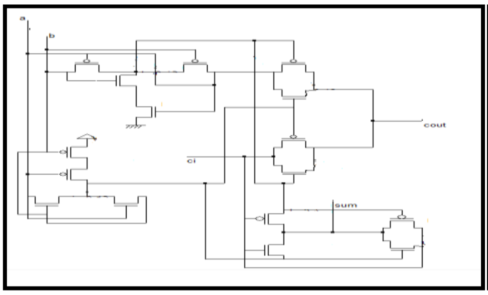
a. Modified Shannon FA [10]



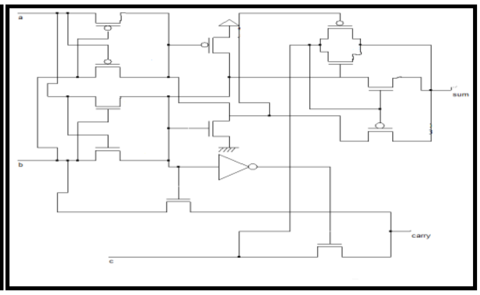
b. Full Adder Using 10T [11]



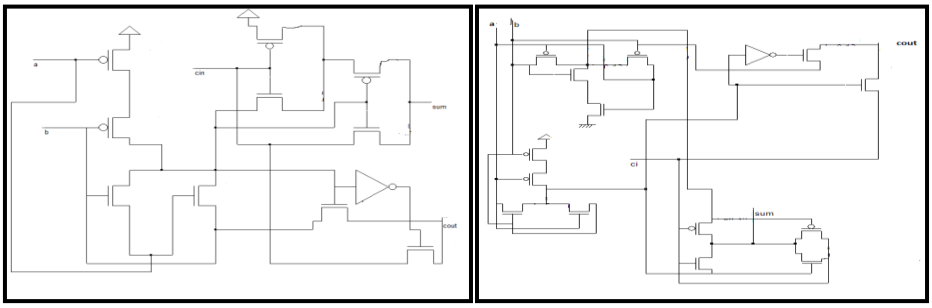
c.Full Adder Using 14T [12]



d. Full Adder Using 16 T [13]



e. Hybrid-I Full adder [14]



f. Proposed Hybrid-A Full adder g. Proposed Hybrid-B Full adder

Fig. 2. Transistor Schematic for different Full Adders and proposed adders

Fig. 2.c shows the Full adder using 14T uses more than one logic style for the implementation and is called as a mixed logic design style. The number of transistors required is 14, and circuit has 3 inputs and 2 outputs, [12] Full adder using 14T generates $A \oplus B$ and use it along with its complement as a select signal to generate the output of the circuit. The advantage of 14T is small transistor count and enhances the non full swing pass transistor. The main drawback is that produce high capacitance values for the input signals. Full adders using 16T are designed with specific kind of XOR and XNOR implementation [13]This full adder has good driving capabilities in fan-out situation with area trade off. Hybrid I and Hybrid II adders are designed using 14T and modified Shannon adders [14].The proposed adders are discussed in detail in the following section.

IV. PROPOSED HYBRID FULL ADDERS

Full adder cell is the basic component of the Multiply Accumulate Unit in DSP processors. Based on the merits and demerits of the existing adder's features, the new Hybrid Full adders are designed. Here, five full adders are modeled using 90nm technology with BSIM. These full adder circuits are analyzed for all the eight combinations of binary inputs with voltage scaling technique (at various supply voltages). From the analyzed circuits, it is found that 14T and Modified Shannon has better the functionality than the other existing circuits. Using 14T and Shannon Modified adders, hybrid adders are designed. The combination of 14T's Sum and Modified Shannon's carry is implemented, called as Hybrid-I, which is shown in Fig. 3.e The width is optimized by transistor sizing to bring the better power consumption without degrading the delay. In order to improve the power, delay and driving capability, Hybrid –A and Hybrid-B Full adders are proposed. Hybrid-A Full adder is designed with 10T Sum and modified Shannon carry which consist of 12 transistors. Hybrid B Full adder is built using low power XOR and XNOR for sum implementation and carry is designed with modified Shannon .It requires 16transistor using pass transistor logic and NMOS transistors. The optimal value of power is obtained by changing the size of the transistor (W/L) and the operating supply voltage V_{dd}. The width of the PMOS and NMOS transistors are alerted from 2.0 µm to 0.1 µm for optimizing Power Delay Product (PDP). These circuits provide good driving capability and better power delay performance.

V. RESULTS AND DISCUSSION

All adder circuits are implemented and simulated using HSPICE with BSIM model at 90nm technology for which parasitic capacitance are considered in the result. A proper simulation test bench is used to simulate a real environment and minimum output load is used for power and delay measurements. Five existing adders and the two new Hybrid adders are simulated and their layouts are developed. The circuit performances are studied using voltage scaling technique (1V, 0.9V & 0.8V). All full adder circuits are analyzed for all the eight combinations of binary input and also for various supply voltages. Hybrid A and Hybrid B Full adder circuits are developed using a combination of 10T, 16 T low power adder and modified Shannon full adder.

Table.1 shows the sum and carry voltage level for all the full adder circuits at V_{dd} =1V, 0.9V, and 0.8V. The area occupied by the adders and number of transistors required to implement the circuit is given in the Table 1.All the full adder circuits are compared at different voltages. The Full adder using Modified Shannon has the lowest number of transistors with the count of 8. It is observed that the voltage loss is high in modified Shannon Full Adder. Hybrid B full adder shows excellent voltage swing at sum and moderate voltage swing at carry outputs. In Table.2 the power and delay for all the full adder circuits at V_{dd}=1V, 0.9V and 0,8V is given. Comparing the performances of the full adder circuits it is observed that the voltage loss is less for Hybrid-B Sum, Hybrid-A has the lowest Delay and Hybrid B has the lowest power consumption for the new design. Comparison of the power and delay of HYBRID A and HYBRID B Full adders with other five adders are shown in Fig .5. All circuit simulations are carried out in 90nm with BSIM model using HSPICE. The power delay product at various V_{dd} of Hybrid adders are shown in Table.3.HYBRID -A adder has very less PDP, which is shown in Fig.6.

Table 1. Sum and Carry voltage level , and Area Analysis of Different Full Adders at Vdd = 1V, at 90 nm Technology

S.no	**Adder**	**No of Transistor**	**Sum (V)**	**Carry(V)**	**Area(** µm2)
1.	Modified Shannon FA	8	0.6	0.6	88.1
2.	FA Using 10T	10	0.8	0.8	124.7
3.	FA Using 14T	14	1.0	1.0	227.7
4.	FA using 16T	16	0.98	0.98	196.0
5.	HYBRID-I FA	14	1.0	0.87	145.9
6.	HYBRID –A FA	12	0.85	0.85	163.1
7.	HYBRID –B FA	16	1.0	0.85	169.6

Table 2. Power and Delay Analysis of Different Full Adders at different voltage at 90nm technology

S.no	**Adder**	**VDD =1V**		**VDD =0.9V**		**VDD =0.8V**	
		Power (µw)	**delay (ps)**	**Power** (µ w)	**delay (ps)**	**Power (µw)**	**Delay (ps)**
1.	Modified Shannon FA[10]	22.03	0.78	18.83	0.97	9.98	1.78
2.	FA Using 10T [11]	1.06	41	0.96	52	0.86	94
3.	FA Using 14T [12]	0.8	10	0.88	11	0.78	13
4.	FA using 16T [13]	0.65	8	0.59	10	0.52	12
5.	HYBRID-I FA [14]	0.61	8	0.55	10	0.48	12
6.	HYBRID –A FA	1.61	0.37	1.45	0.72	1.20	0.95
7	HYBRID –B FA	0.67	6	0.61	7	0.53	9

Table 3. Power Delay Product Analysis of Different 1 Bit Full Adder At Vdd =1V, 0.9V and 0.8V

Sno	**Adder**	**Power delay product**		
		VDD 1 V (e-18)	**VDD 0.9 V (e-18)**	**VDD 0.8 V (e-18)**
1.	Modified Shannon FA	17.18	17.46	17.76
2.	FA Using 10T	43.46	49.92	88.84
3.	FA Using 14T	8.0	9.68	10.14
4.	FA using 16T	5.2	5.9	6.24
5.	HYBRID-I FA	4.88	5.5	5.76
6.	HYBRID –A FA	0.59	1.04	1.14
7.	HYBRID –B FA	4.02	4.27	4.77

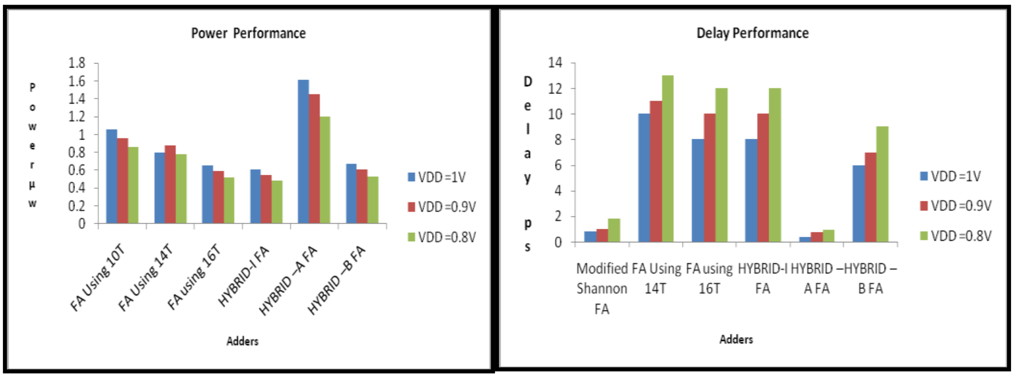


Fig. 5.a. Power and Delay performance of various Full Adders

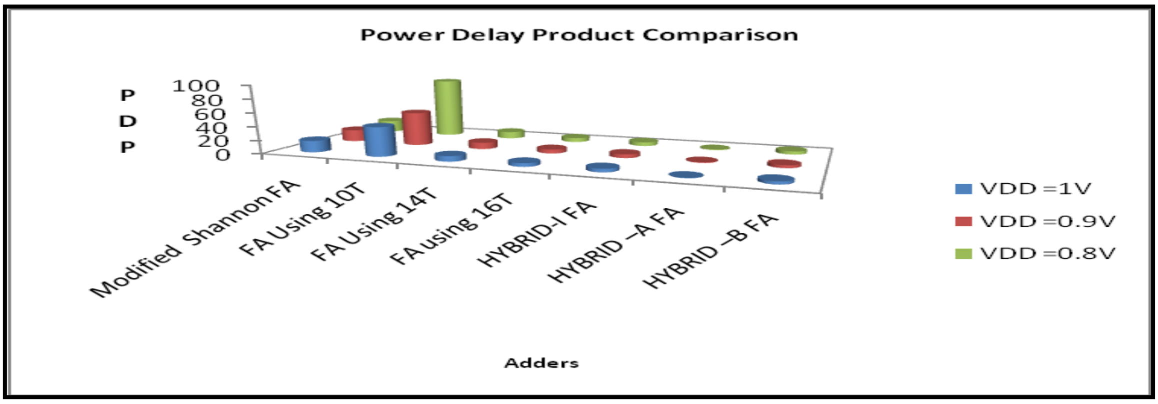


Fig. 5.b. Power Delay Product performance of various Full Adders

VI. CONCLUSION

In this paper, HYBRID- A and HYBRID -B full adders are proposed for data path circuit (MAC unit) for low power DSP application. The proposed circuit uses full adder using 10T, 16 T and Modified Shannon circuits. The existing five adders and two proposed full adder circuits are implemented and simulated in HSPICE using BSIM model at 90nm Technology .The power, voltage level, delay and PDP values of all the full adder circuits are analyzed. The optimal value of power and PDP is obtained by transistor sizing and voltage scaling. The performance analysis of various full adders at Vdd=1V, 0.9V, 0.8V using 90nm technology are carried out. It is observed from the simulated results that the proposed circuit has the lowest Delay, Voltage Loss and Power Consumption with reduction in area occupied. The functionality test of different full adders at Vdd=1V, 0.9V, 0.8V using 90nm technology are also verified. All 8 combinations of Binary input are tested for each circuit. It is found that HYBRID- B has the better power consumption compared with Hybrid -A Full Adder and delay performance is good in the Hybrid -A circuits. At low voltage level (Vdd =1), HYBRID-A adder has very less power delay product (nearly 4-95% of improvement) compared with other adders with better area occupation. Here, all the circuits are simulated using the BSIM model at 90nm technology. This can also be tried for other models of submicron technology less than 65nm.Therefore these Hybrid adders can be utilized for low power high performance applications.

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