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Power Quality Enhancement through Dynamic Voltage Restorer using SRF Theory for Balanced and Unbalanced Loads

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Abstract:- Power quality is certainly a major concern in the present era, it becomes especially important with the introduction of sophisticated devices, whose performance is very sensitive to the quality of power supply. Voltage sag is one of the severe power quality problems. This report addresses all the different aspects related to voltage sag problem, such as its types, consequences and mitigation.
At present, a wide range of very flexible controllers, which capitalize on newly available power electronics components, are emerging for custom power applications. Among these, the distribution static compensator (D-STATCOM) and the dynamic voltage restorer (DVR) are most effective devices, both of them based on the VSC principle.

A simple generalized algorithm based on basic synchronous reference-frame theory has been developed for the generation of instantaneous reference compensating voltages for controlling a DVR. This algorithm makes use of the fundamental positive sequence phase voltages extracted by sensing only two unbalanced and/or distorted line voltages. The algorithm is general enough to handle linear as well as nonlinear loads. The compensating voltages when injected in series with a distribution feeder by three single-phase H-bridge voltage-source converters with a constant switching frequency hysteresis band voltage controller tightly regulate the voltage at the load terminals against any power quality problems on the source side. A capacitor-supported DVR does not need any active power during steady-state operation because the injected voltage is in quadrature with the feeder current.

MATLAB SIMULINK has been used in this project to perform the modeling and analysis of such controllers Comprehensive results is presented to assess the performance of each device as a potential custom power solution.

Index Terms:- Dynamic Voltage Restorer (DVR), Hysteresis Band Controller, Nonlinear load, Voltage-Source Converter (VSC).

I. INTRODUCTION

Voltage **sags** and swells have been **one** of **the** most important power quality problems. Voltage sag is a momentary decrease in the rms voltage magnitude lasting between half a cycle to few cycles. Voltage fluctuations, sags and swells interrupt and disturb the sensitive manufacturing processes [1].When fault occurs in a distribution network, a sudden voltage dip will appear on adjacent load feeders. With the DVR installed on a critical load feeder, the line voltage is restored to its nominal value within the response time of a few milliseconds thus avoiding any power disruption to the load.

The concept of custom power has been proposed recently using advance power electronic equipment to ensure a high quality of supply [12]. The series power quality compensator is inserted between the power supply and the consumer. It isolates the harmonics on the system side and injects a compensation voltage to keep the consumer side voltage constant [11].

A power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages is called a dynamic voltage restorer [10]. The basic task of the DVR is to maintain the magnitude of the appliance voltage phasor $|V_a|$=1p.u. [10].It injects three single phase alternating voltages in series and in synchronism with up stream voltages in the distribution system. The amplitude and phase angle of injected voltages are flexibly controlled depending on the real and reactive power exchange that is required [13]. The injected voltages are introduced into the distribution system through an injection transformer connected in series with the distribution feeder.

The main functions of the injection transformer include voltage boost and electrical isolation[14].The reactive power exchanged between the restorer and the distribution system is internally generated by the restorer without ac passive reactive components [11].DVR is preferred because of the cost and size considerations [9]. For higher power sensitive loads, where the energy storage capabilities of uninterruptible power supplies (UPS)

become very costly, the dynamic voltage restorer (DVR) shows promise in providing a more cost effective solution. The DVR can be implemented both at a low voltage (LV) level as well as at a medium voltage (MV) level and gives an opportunity to protect high power applications from voltage sags. DVR is useful in cases where numerous sensitive loads are connected to the same feeder [8].

Different topologies of the DVR are discussed in [16]. The DVR supported by a capacitor has become popular as a cost-effective solution for the protection of sensitive loads from the supply-side voltage quality problems. Currently, most of the research is on DVR dealing with the protection of balanced linear load; however, there are a few which are related to the protection of unbalanced and nonlinear loads [15].

In this paper, a simple generalized control algorithm for the self-supported DVR is developed based on the basic SRFT.This novel algorithm makes use of the fundamental positive sequence phase voltages extracted by sensing only two unbalanced and/or distorted line voltages. The algorithm is general enough to handle linear as well as nonlinear loads. The self supported DVR maintains balanced sinusoidal load voltage with desired magnitude against any supply voltage quality problem even when the load is unbalanced and nonlinear in nature. The algorithm based on instantaneous symmetrical components along with the complex Fourier transform to protect unbalanced and nonlinear load discussed in [15] is computationally demanding and requires huge memory space. The approach discussed here is comparatively simple as it needs only the extraction of the fundamental positive-sequence phase terminal voltages, thus making it computationally simpler with the least memory requirement. The proposed fundamental positive-sequence extractor requires the sensing of only two line voltages of supply. This reduces the analog-to-digital converter (ADC) requirements of a digital controller and corresponding sensing element. Moreover, it is able to extract three fundamental positive-sequence phase voltages irrespective of the distribution system configuration such as three-phase, fourwire or three-phase, three-wire system where the neutral is not available for sensing phase voltages. In this paper, a hybrid structure of the self-supported DVR is considered in which a shunt capacitor filter is used to provide the low impedance path for higher order harmonics of the load currents [15]. The DVR is realized by three single-phase H-bridge VSCs with a constant switching frequency hysteresis band voltage controller [17].

II. CONTROL STRATEGY OF DVR

The major objective of the control strategy is to ensure that the load bus voltages remain balanced and sinusoidal (positive sequence). Since the load is assumed to be balanced and linear, the load currents will also remain balanced (positive sequence) and sinusoidal. An additional objective is to ensure that the source current remains in phase with the fundamental frequency component of the PCC voltage. This requires that the reactive power of the load is met by the DVR. It is also possible to arrange that DVR supplies a specified fraction of the reactive power required by the load

The practical implementation of a DVR using three single-phase H-bridge VSCs along with a common dc capacitor is discussed later. The energy storage device is a capacitor, so the following condition is stipulated on the DVR.

• The DVR should not supply any real power in steady state. This implies that, in steady state, the phase difference between instantaneous DVR voltages and instantaneous line currents must be 90◦.

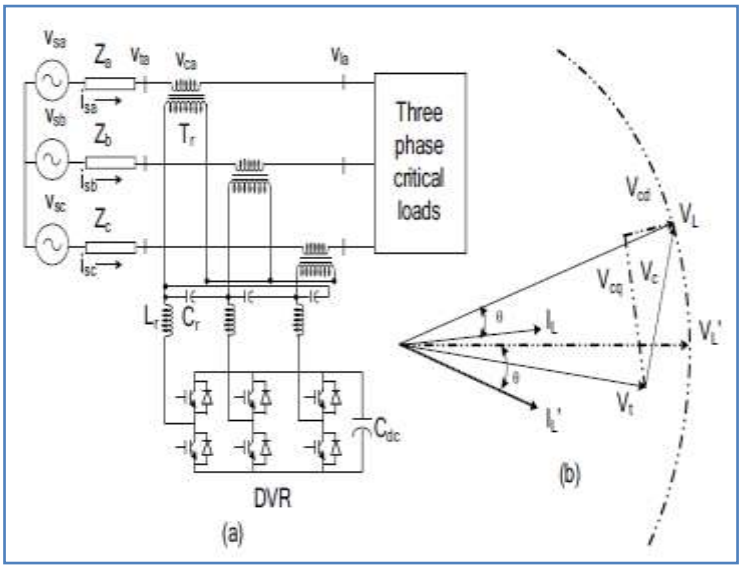

Fig. 1. DVR configuration

Here, three single phase full bridge converters are connected to a common DC bus. The sine PWM technique is used to control the DVR. The DC bus voltage is held by the capacitor Cdc. Since no energy source is connected, the net real power exchanged by the DVR is zero in steady state, if the losses are neglected.

However, to stabilize the operating point, a DC bus voltage control loop is necessary. The phasor diagram shows the current phasor is in phase with the voltage phasor VP (PCC voltage). The source and the load bus voltage phasor are also shown here. Á is the power factor angle of the load. The voltage injected by the DVR (VC) ensures that the current IS is in phase with VP. From the phasor diagram, the d-q components of the load bus voltage are given by

$V_{Ld} = V_P + V_{Cd}$ --(1)

The Synchronous Reference Frame (SRF) approach is used to generate the reference voltages for the DVR.

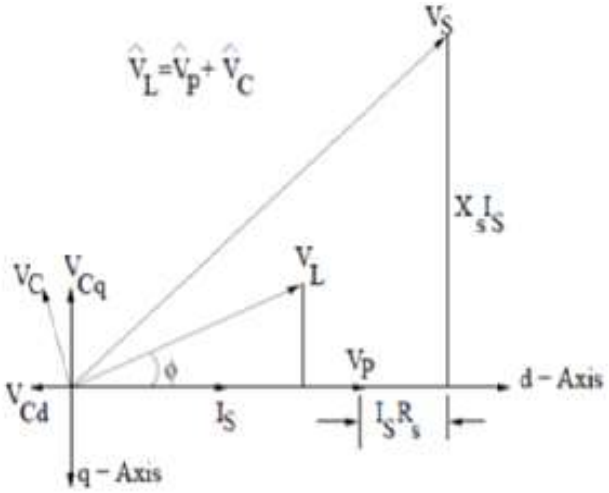

Fig 2 Phasor diagram for the system

Fig. 2 shows the control scheme using SRF. The PCC voltage VPa, VPb and VPc are transformed into d-q components using the following equations.

$$\begin{bmatrix} V_{P\alpha} \\ V_{P\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{Pa} \\ V_{Pb} \\ V_{Pc} \end{bmatrix} \qquad (2)$$

$$\begin{bmatrix} V_{Pd} \\ V_{Pq} \end{bmatrix} = \begin{bmatrix} \cos\omega_0 t & -\sin\omega_0 t \\ \sin\omega_0 t & \cos\omega_0 t \end{bmatrix} \begin{bmatrix} V_{P\alpha} \\ V_{P\beta} \end{bmatrix}$$

Where ω_0 is the operating system frequency. In the synchronously rotating reference frame, the positive sequence, fundamental frequency components are transformed into DC quantities. The negative sequence components and harmonic components (irrespective of the sequence) are transformed into oscillating quantities of frequency (fdq) given by

$$fdq = fabc * 1 \qquad (3)$$

Where fabc is the frequency of the positive or negative sequence components in the phase coordinates. The sign associated with the second term in the R.H.S. of Equation is negative for positive sequence components and positive for negative sequence components. Note that zero sequence components in the phase coordinates do not contribute to d-q components.

III. SRF BASED EXTRACTION OF REFERENCE PARAMETERS

1. Computation of reference Load Voltages

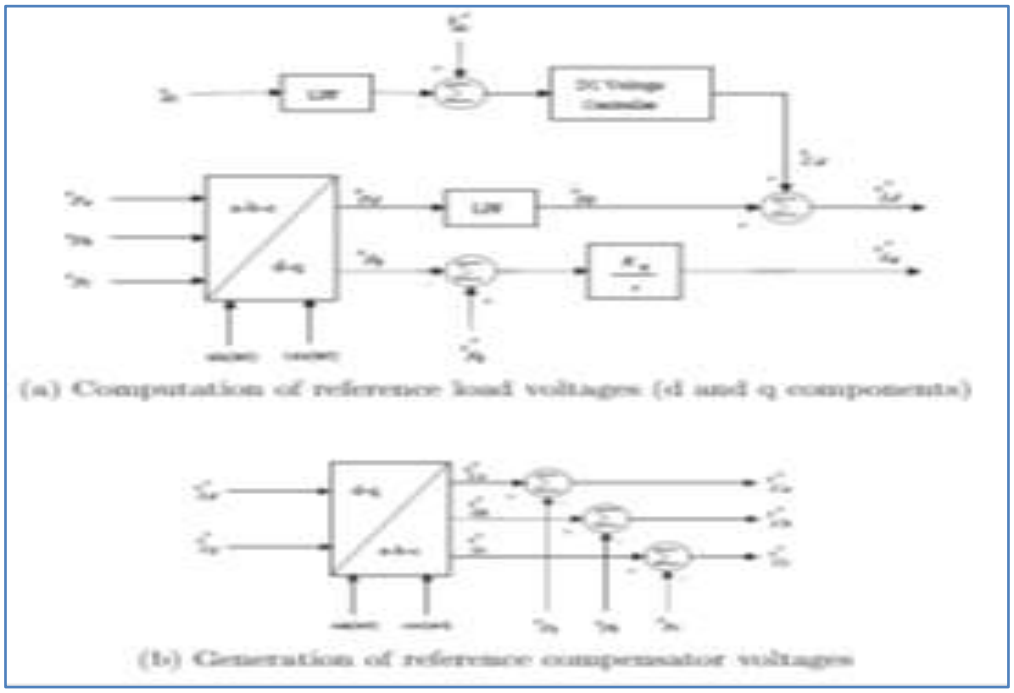

Fig 3 Block diagram for computing reference load voltages

The synchronously rotating reference frame is synchronized with the source current (IS) using a PLL. Therefore, the components Vpd and Vpq are the active and reactive components of the PCC voltage. The DC components in Vpd and Vpq are extracted by using a low pass filter Thus,

$$\begin{aligned} V_{Ca}^{*} &= V_{La}^{*} - V_{Pa} \\ V_{Cb}^{*} &= V_{Lb}^{*} - V_{Pb} \\ V_{Cc}^{*} &= V_{Lc}^{*} - V_{Pc} \end{aligned} \quad \text{---4}$$

$$\begin{bmatrix} \bar{V}_{Pd} \\ \bar{V}_{Pq} \end{bmatrix} = G(s) \begin{bmatrix} V_{Pd} \\ V_{Pq} \end{bmatrix} \quad \text{---5}$$

Where are the DC components. From Equation we derive the reference for the active component of the load voltage (VLd) as

$$V_{Ld}^{*} = \bar{V}_{Pd} + V_{Cd} \quad \text{-----6}$$

Where, Vcd is obtained as the output of the DC voltage controller (with a proportional gain Kp). A second order Butterworth low pass filter is used in the feedback path of the DC voltage controller to filter out high frequency ripple in the DC voltage signal. In steady state, Vpq = 0 and . These two conditions can be met by arranging

$$V_{Lq}^{*} = \frac{K_q}{s} \cdot V_{Pq} \quad \text{----7}$$

Kq is chosen to optimize the controller response. From the reference values of Vld and Vlq we can obtain the desired load voltages in phase coordinates from the following equations.

Finally, the reference voltages for the DVR are given by

$$\begin{bmatrix} V_{L\alpha}^* \\ V_{L\beta}^* \end{bmatrix} = \begin{bmatrix} \cos\omega_0 t & \sin\omega_0 t \\ -\sin\omega_0 t & \cos\omega_0 t \end{bmatrix} \begin{bmatrix} V_{Ld}^* \\ V_{Lq}^* \end{bmatrix} \quad \text{--8}$$

$$\begin{bmatrix} V_{La}^* \\ V_{Lb}^* \\ V_{Lc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{L\alpha}^* \\ V_{L\beta}^* \end{bmatrix}$$

It is to be noted that the DVR will not be able to compensate for the harmonics in the load current produced by nonlinear loads. This would require shunt connected DSTATCOM. When both load compensation and harmonic isolation (from the source) are required, then Unified Power Quality Conditioner (UPQC), to be described in the next section, is the appropriate device for improvement of power quality. UPQC also helps in regulating the load bus voltage in the presence of large variations (sag or swell) in the supply voltages. The DVR with capacitor on the DC side has the limitations of having to inject only reactive voltage in steady state. This may not be able to compensate fully large variations in the PCC voltage.

2. Computation of reference Currents

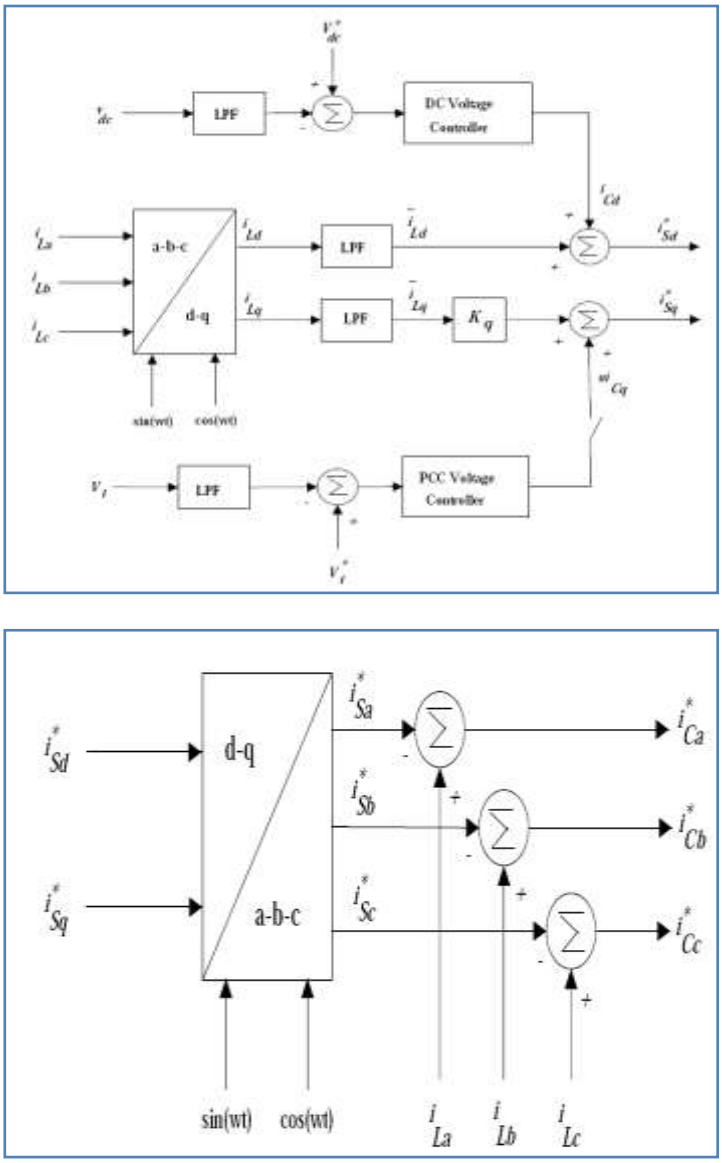

Fig 4 Block diagram for computing reference currents

The block diagram of the control scheme to generate the reference values of the compensator currents is shown in Fig. 4.The desired source currents (in d-q components) are obtained as

$$i_{Sd}^{*} = \bar{i}_{Ld} + i_{Cd}$$

- -----10

$$i_{Sq}^{*} = K_q \bar{i}_{Lq} + u i_{Cq}$$

- ------11

where ILd and ILq are the average values of the d- and q- axis components of the load current, icd is the output of the DC voltage controller and icq is the output of the AC voltage controller (if the bus voltage (Vt) is to be regulated). u is a logical variable equal to (a) zero if PF is to be regulated and (b) one if bus voltage is to regulated. Kq = 1 in the latter case. When PF is to be controlled, Kq is determined by the required power factor as follows

$$K_q = \frac{Q_S^{*}}{\bar{Q}_L} \qquad \text{-12}$$

where Q¤S is the reference reactive power supplied by the source (at PCC) and ¹QL is the average reactive power (at fundamental frequency) defined by

$$\bar{Q}_L = |V_t| \bar{i}_{Lq} \qquad \text{--13}$$

For unity power factor, Q¤S = 0 and Kq = 0. The average values of iLd and iLq are obtained as the outputs of two identical low pass filters and are defined as

$$\begin{bmatrix} \bar{i}_{Ld} \\ \bar{i}_{Lq} \end{bmatrix} = G(s) \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} \qquad \text{---14}$$

where G(s) is chosen as the transfer function of a 2nd order Butterworth low pass filter (with a corner frequency of 30 Hz). The d-q components are computed from the following relations

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \qquad \text{--15}$$

where the (α β)components are obtained

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \qquad \text{----16}$$

The reference vector of source currents is given by

$$\begin{bmatrix} i_{Sa}^{*} \\ i_{Sb}^{*} \\ i_{Sc}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{S\alpha}^{*} \\ i_{S\beta}^{*} \end{bmatrix} \qquad \text{----17}$$

where the (α β) currents are given by

$$\begin{bmatrix} i^*_{S\alpha} \\ i^*_{S\beta} \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} i^*_{Sd} \\ i^*_{Sq} \end{bmatrix}$$

--18

Note that! Is the supply frequency expressed in radians/sec. The unit vectors sin !t and cos !t are obtained from Phase-Locked Loop (PLL) which is locked to the PCC voltage.

IV. DVR CONTROL STRATEGY

The proposed algorithm is based on the estimation of reference supply currents. It is similar to the algorithm for the control of a shunt compensator like DSTATCOM for the terminal voltage regulation of linear and nonlinear loads [6]. The proposed control algorithm for the control of DVR is depicted in Fig 5

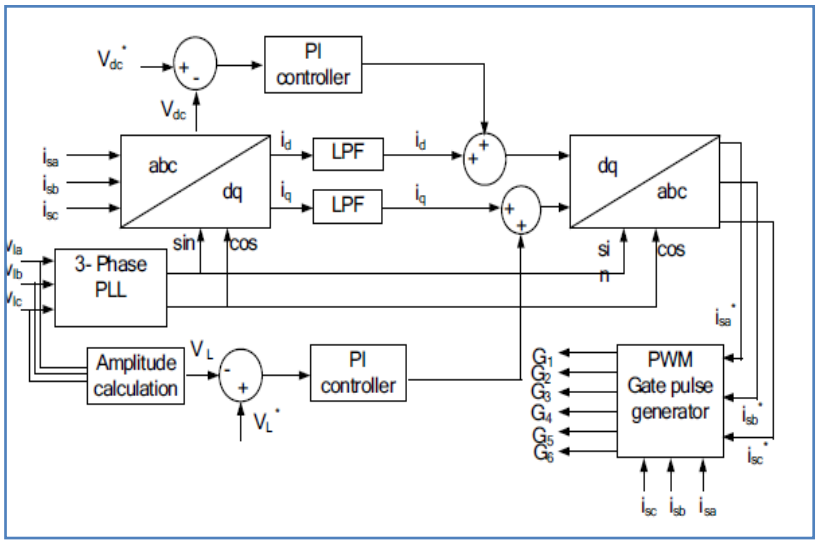

Fig 5 Control scheme of the DVR

The series compensator known as DVR is used to inject a voltage in series with the terminal voltage. The sag and swell in terminal voltages are compensated by controlling the DVR and the proposed algorithm inherently provides a self-supporting dc bus for the DVR. Three-phase reference supply currents (isa*, isb*,isc*) are derived using the sensed load voltages (vla, vlb, vlc), terminal voltages (vta, vtb, vtc) and dc bus voltage (vdc) of the DVR as feedback signals. The synchronous reference frame theory based method is used to obtain the direct axis (id) and quadrature axis (iq) components of the load current. The load currents in the three-phases are converted into the d-q-0 frame using the Park's transformation as,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \quad (19)$$

A three-phase PLL (phase locked loop) is used to synchronies these signals with the terminal voltages (vta, vtb, vtc). The d-q components are then passed through low pass filters to extract the dc components of id and iq. The error between the reference dc capacitor voltage and the sensed dc bus voltage of DVR is given to a PI (proportional-integral) controller of which output is considered as the loss component of current and is added to the dc component of id. Similarly, a second PI controller is used to regulate the amplitude of the load voltage (Vt). The amplitude of the load terminal voltage is employed over the reference amplitude and the output of PI controller added with the dc component of iq. The resultant currents are again converted into the reference supply currents using the reverse Park's transformation. Reference supply currents (isa*, isb*,isc*) and the sensed supply currents (isa, isb, isc) are used in PWM current Controller to generate gating pulses for the

switches. The PWM controller operates at a frequency of 10 kHz and the gating signals are given to the three-leg VSC for the control of supply currents.

V. SIMULATION IN MATLAB

The DVR is modeled and simulated using the MATLAB and its Simulink and Power System Block set (PSB) toolboxes. The MATLAB model of the DVR connected system is shown in Fig. 5. The three-phase source is connected to the three-phase load through series impedance and the DVR. The considered load is a lagging power factor load. The VSC of the DVR is connected to the system using an injection transformer.

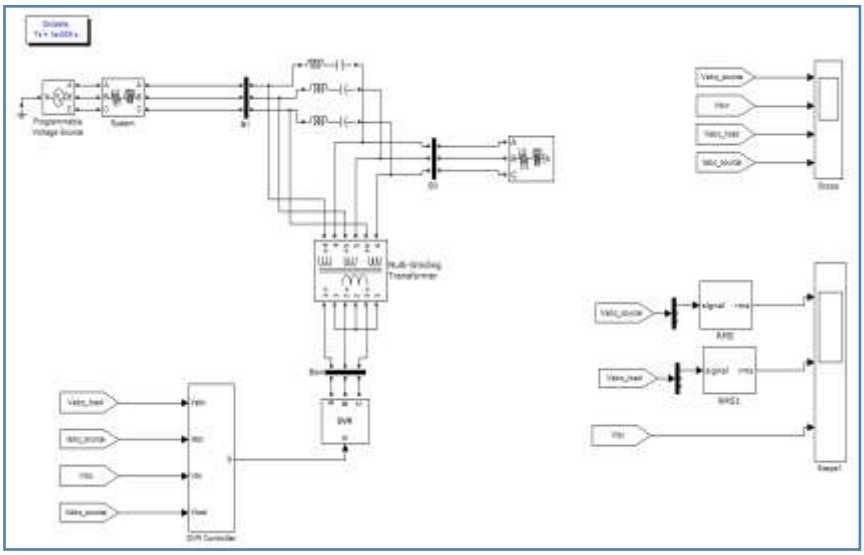

Fig 6 MATLAB based model of the three-phase DVR connected system.

In addition, a ripple filter for filtering the switching ripple in the terminal voltage is connected across In the terminals of the secondary of the transformer. The dc bus capacitor of DVR is selected based on the transient energy requirement and the dc bus voltage is selected based on the injection voltage level. The dc capacitor decides the ripple content in the dc voltage. The system data are given in Appendix.

The proposed control algorithm is modeled in MATLAB as shown in Fig.5.3. The reference supply currents are derived from the sensed load voltages, supply currents and dc bus voltage of DVR. The output of the PI controller used for the control of dc bus voltage of DVR is added with the direct axis component of current. Similarly, the output of the PI controller used for the control of the amplitude of the load voltage is added with the quadrature axis component.

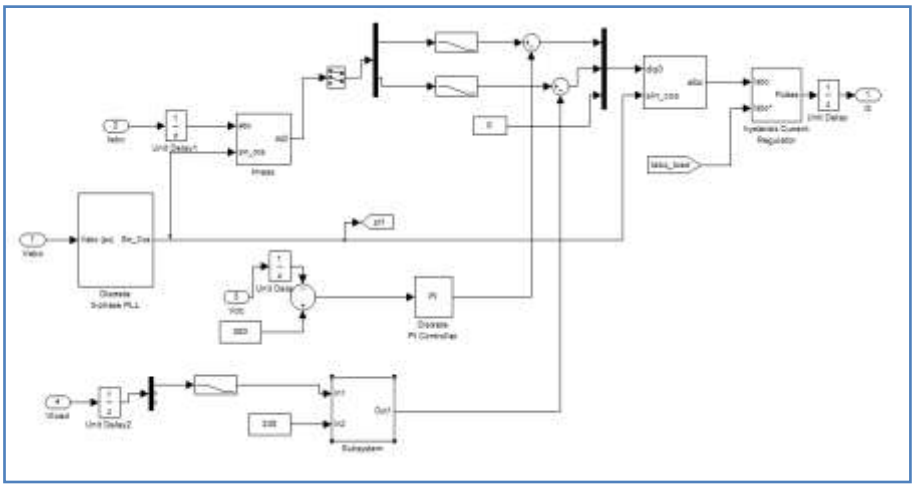

Fig7 MATLAB based model of the proposed control method.

Of the supply current. A pulse width modulation (PWM) controller is used over the error between reference supply currents and sensed supply currents to generate gating signals for the IGBT's (insulated gate bipolar transistors) of the VSC of DVR.

Voltage Sag

The proposed control scheme of DVR is verified through simulation using MATLAB software along with its Simulink and Power System Blockset (PSB) toolboxes. The DVR is tested under different operating conditions like sag (Fig.8) and swell (Fig. 9) at the terminal voltages (Vta, Vtb, Vtc). In Fig. 8, the terminal voltage has sag of 30% with a magnitude at 70% of rated value at 0.22 sec and occurs up to 0.32 sec. The DVR injects fundamental voltage (Vc) in series with the terminal voltages (Vla, Vlb, Vlc). The load voltage is maintained at the rated value. The terminal voltage (Vt), supply current (is), amplitude of terminal voltage (Vt) the amplitude of load voltage (VL) and the dc bus voltage (Vdc) of DVR are also shown in the Fig.8. It is observed that the dc bus voltage of DVR is maintained at reference value.

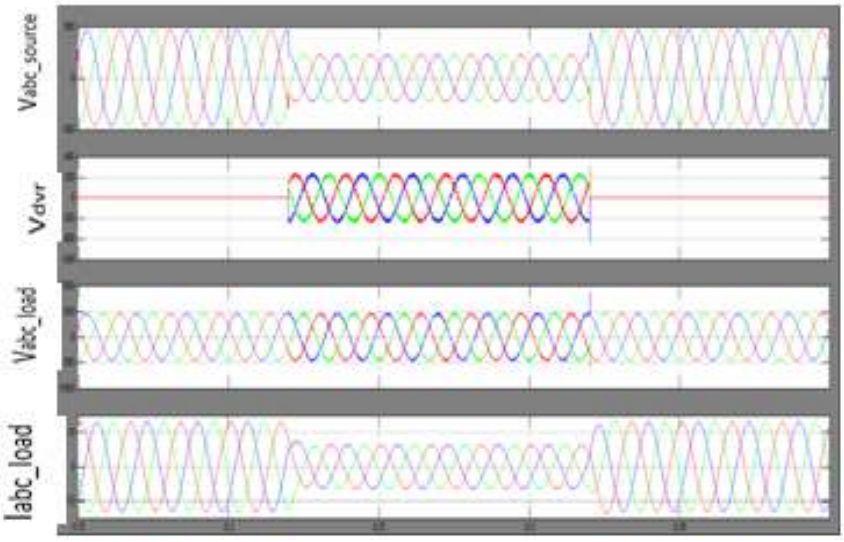

Fig 8 Dynamic behavior of DVR for voltage sag compensation.

Voltage Swell

Similarly, in Fig.9, a swell in terminal voltage (Vt) has occurred at 0.22 sec up to 0.32 sec and the load voltage (VL) is observed to be satisfactory due to the proper voltage injection by the DVR. The load voltage (VL) is maintained at the rated value. The terminal voltage (Vt) supply current (Is), the amplitude of terminal voltage (Vt), the amplitude of the load voltage (VL) and the dc bus voltage (Vdc) of DVR are also shown in the Fig 9. It is observed that the dc bus voltage of DVR is maintained at reference value, though perturbation is occurring during transients.

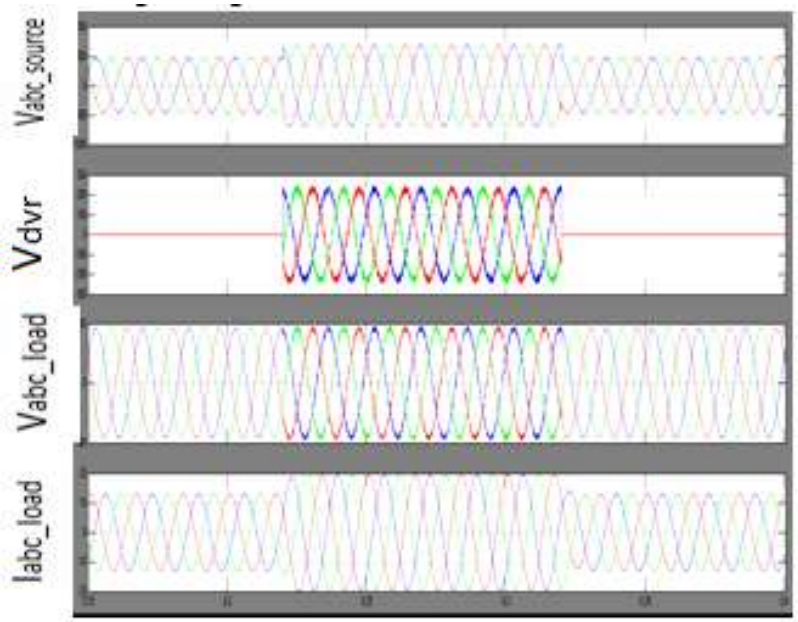

Fig 9 Dynamic behaviors of DVR for voltage swell compensation.

VI. CONCLUSION

A new control strategy based on current mode control for Dynamic Voltage Restorer (DVR) has been proposed to mitigate the power quality problems in the terminal voltages. The DVR is controlled indirectly by controlling the supply current. The reference supply currents are estimated using the sensed load terminal voltages and the dc bus voltage of DVR. The control scheme is based on synchronous reference frame theory (SRFT) for the operation of a capacitor supported DVR. The proposed control scheme of DVR has been validated the compensation of sag and swell in terminal voltages. The performance of the DVR has been found very good to mitigate the voltage power quality problems. Moreover, it has been found capable to provide self-supported dc bus of the DVR through power transfer from ac line at fundamental frequency.

VII. FUTURE SCOPE

Finally I would conclude that, the new control strategy based on current mode control for DVR is proposed to mitigate the power quality problems in the supply voltage. The DVR is controlled indirectly by controlling the supply current. In future this can be implemented by using a new control strategy of an Adaline (Adaptive linear element) Artificial Neural Network (ANN) can be used to control a capacitor supported DVR for power quality improvement.

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