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Enhancement of Power Quality with Multifunctional D-STATCOM Operated under Stiff Source for Induction Motor Applications

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Abstract:- Electricity plays an important role in the economic development and technology advancement throughout the world. The quality and reliability of power supplies relates closely to the economic growth of a country. However, power quality disturbances such as sags, swells, flicker, harmonics, voltage imbalance etc., create a lot of problems in achieving a reliable and quality power supply. These power quality problems are very common in the electrical distribution systems. The poor voltage or reactive power compensation can be minimized or overcome by using FACTS device such as DSTATCOM. In this paper proposes a new control-algorithm-based DSTATCOM topology for voltage regulation even under stiff source. It is achieved by connecting a suitable external inductor in series between the load and the source point. The point of common coupling (PCC) will be the point where external inductor and source are connected. A DSTATCOM connected at the load terminal provides voltage regulation at the load terminal during voltage disturbances and protects induction machine drive. The simulation results are presented by using MATLAB/SIMULINK software**.**

Index Terms:- *DSTATCOM, multifunctional, stiff source, power factor, voltage regulation, induction machine drive* **.**

I. INTRODUCTION

Power quality and reliability in distribution systems have been attracting an increasing interest in modern times and have become an area of concern for modern industrial and commercial applications. Introduction of sophisticated manufacturing systems, industrial drives, precision electronic equipments in modern times demand greater quality and reliability of power supply in distribution networks[7].The distribution static compensator is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the presence of feeder impedance and nonlinear loads distorts the terminal voltage (PCC) and source currents. The load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives better results [2]. The switching frequency components in the terminal voltages and source currents are eliminated by using state feedback control of shunt filter capacitor. in this situation, DSTATCOM should operate in CCM. However, due to grid faults, source voltage (stiff or non-stiff) can change at any time and then VCM operation is required. DSTATCOM regulates the load voltage by indirectly regulating the voltage across the feeder impedance. When a load is connected to nearly a stiff source, feeder impedance will be negligible [1]–[4]. Under these circumstances, DSTATCOM can not provide sufficient voltage regulation at the load terminal [9].

In this paper a new control algorithm based multifunctional DSTATCOM proposed to protect the load from voltage disturbances under stiff source. It has been achieved by placing an external series inductance of suitable value between the source and the load. Point of common coupling (PCC) will be the point where external inductor and source are connected. DSTATCOM, connected at the load terminal, provides voltage regulation by indirectly regulating the voltage across the external inductor. Proposed control algorithm to obtain variable reference load voltage is formulated as a function of the desired source current. This voltage indirectly controls the current drawn from the source for a permissible range of source voltage. There fore, the control algorithm makes source currents balanced, sinusoidal, and in phase with respective source voltages during normal operation. During voltage disturbances, a constant voltage is maintained at the load terminal. Hence, proposed topology and control algorithm make compensator multifunctional so that it provides fast voltage regulation at load terminal and additionally provides advantages of CCM while operating in VCM.

II. DSTATCOM CONFIGURATION

A neutral point clamped voltage source inverter (VSI) topology is chosen as it provides independent control of each leg of the VSI [7]. A single phase equivalent circuit of DSTATCOM in distribution network is shown in Fig. 1.VSI represented by u V dc is connected to load terminal through an LC filter ($L_f - C_{fc}$).

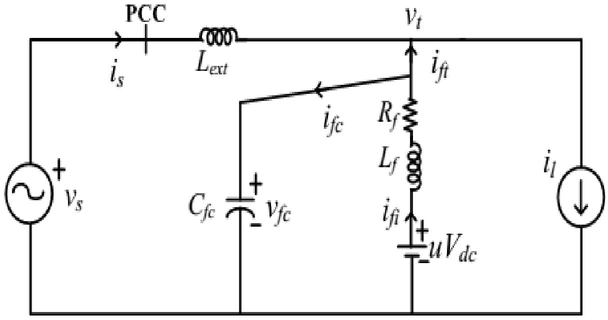

Fig.1.Single phase equivalent circuit of DSTATCOM in distribution network.

The load terminal is connected to the PCC through an external series inductance L_{ext}. V_{dc} is the voltage maintained across the each dc capacitor and u is a control variable which can be +1 or -1 depending upon switching state. I_{fi}, i_{ft}, and i_{fc} are currents through VSI, DSTATCOM, and C_{fc} respectively. V_s and V_t are source and load voltages respectively. Loads have both linear and nonlinear elements with balanced or unbalanced features. Load and source currents are represented by I and is respectively.

III. SELECTION OF EXTERNAL INDUCTOR

Under normal operation, external impedance (Z_{ext}) does not have much importance, whereas it plays a critical role during voltage disturbances. The value of external impedance is decided by the rating of the DSTATCOM and amount of sag to be mitigated. At any time, the source current in any phase by assuming balanced source voltage is given as

$$\bar{I}_s = \frac{V_s\angle 0 - V_t\angle -\delta}{R_{ext} + jX_{ext}} \qquad (1)$$

Where V_s, V_t, R_{ext}, X_{ext}, and δ are the RMS source voltage, RMS load voltage, external resistance, external reactance, and load angle respectively. For most practical case $X_{ext} >> R_{ext}$. As a worst case design the reactive source current ($I_m[\bar{I}_s]$) which is supplied by the compensator, will be maximum when is minimum. For this, source will supply only losses in the VSI. Therefore, it will be very small. Hence, $I_m[\bar{I}_s]$) is given as

$$I_m[\bar{I}_s] = \frac{V_t - V_s}{X_{ext}} \qquad (2)$$

During voltage disturbances, the aim is to protect the sensitive loads with focus is on to improve the DSTATCOM capability to mitigate deep sag. Therefore, keeping it into account, the load voltage during voltage sag is taken as 0.9 pu (per unit) which is sufficient to protect the load. Assuming that the reactive current that a compensator can inject is 20 A and load needs to be protected from sag of 40%, then the value of external reactance is found to be

$$X_{ext} = \frac{0.9 - 0.6}{20} \times 230 = 3.45\Omega \qquad (3)$$

External reactance of 3.45 that corresponds to an inductance of 11 mH for a 50 Hz supply is used.

IV. P ROPOSED CONTROL ALGORITHM

Proposed control algorithm aims to provide fast voltage regulation at the load terminal during voltage disturbances while retaining the advantages of CCM during normal operation. Firstly, currents that must be drawn from the source to get advantages of CCM are computed. Using these currents, magnitude of voltages that need to be maintained at load terminal is computed. If this voltage magnitude lies within a permissible range then same voltage is used as reference voltage to provide advantages of CCM. If voltage lies outside the permissible range, it is a sign of voltage disturbance and a fixed voltage magnitude is selected as reference voltage. A two loop controller, whose output is load angle, is used to extract load power and VSI losses from the source. Finally, a discrete model is derived to obtain switching pulses. All these steps are presented in detail in this section.

A. Computation of Reference Voltage Magnitude (V_t^*)

During normal operation, load voltage must be regulated in such a way that following advantages provided by CCM operation are achieved:

1. Source currents are balanced and sinusoidal.
2. Unity power factor (UPF) at PCC.
3. Source supply load average power and VSI losses.

To achieve all aforementioned objectives, instantaneous symmetrical component theory [15] is used to get reference source currents. DSTATCOM makes the load voltages balanced and sinusoidal, but still may contain some switching harmonics which will give unacceptable reference source currents when directly used. Therefore, positive sequence component of load voltages (v^+_{ta1}, v^+_{tb1}, and v^+_{tc1}) are extracted and used to compute reference source currents (i^*_{sa}, i^*_{sb}, and i^*_{sc}) as follows:

$$i^*_{sa} = \frac{v^+_{ta}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$
$$i^*_{sb} = \frac{v^+_{tb}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$
$$i^*_{sc} = \frac{v^+_{tc1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right) \qquad (4)$$

Where, $\Delta^+_1 = \sum_{j=a,b,c}(V^+_{tj1})^2$, P_{lavg} is average load power and is calculated using a moving average filter (MAF). Total losses in the inverter, P_{loss}, computed using a PI controller, helps in maintaining averaged dc link voltage ($V_{dc1} + V_{dc2}$) at a predefined reference value ($2V_{dcref}$) by drawing a set of balanced currents from the source and is given as follows:

$$P_{loss} = K_{pdc}\, e + K_{idc} \int e\, dt \qquad (5)$$

Where, K_{pdc}, K_{idc}, and $e = 2V_{dcref} - (V_{dc1} + V_{dc2})$ are proportional gain, integral gain, and voltage error of the PI controller respectively. The reference currents to be drawn from the source are computed using (4), reference voltages at the load terminal can be derived. Applying KVL in the circuit shown in Fig. 1

$$\bar{V} = \bar{I}_s Z_{ext} + \bar{V}_t \qquad (6)$$

Source voltage and source current will be in phase for the UPF operation. Also, source voltage is taken as reference. Therefore

$$V_s = I_s(R_{ext} + j\,X_{ext}) + V_t\angle\dot{-}\delta\,.$$

From the above equation, the load voltage can be computed as follows:

$$V_t = \sqrt{(V_s - I_s R_{ext})^2 + (I_s X_{ext})^2} \qquad (7)$$

Based on standards, load voltage has a permissible range of variations between 0.9 to 1.1 Pu. Therefore, as long as V_t, obtained using (7) lies between 0.9 to 1.1 Pu, is used as reference load voltage (V^*_t) and the advantages of CCM operation are achieved. Here, V_t is indirectly controlled by the desired source current. During sag and swell, the load voltage magnitude will be between 0.9 to 0.1 Pu and 1.1 to 1.8 Pu respectively for half cycle to 1 minute [16]. Therefore, reference load voltage magnitudes are set to 0.9 Pu and 1.1 Pu during sag and swell respectively. The reason to keep load voltages at these values is to maximize the DSTATCOM disturbance withstanding ability while keeping load voltage at the safe limits for satisfactory operation. Therefore, following conclusions can be drawn:

$$\begin{aligned}&If\ 0.9\,pu \le V_t \le 1.1\,pu \text{ then } V^*_t = V_t\\ &\text{Else} \quad \text{If } V_t > 1.10 \text{ pu then } V^*_t = 1.1 \text{ pu}\\ &\quad \text{else if } V_t < 0.9 \text{ pu then } V^*_t = 0.9 \text{ pu}\end{aligned} \qquad (8)$$

B. Computation of Load Angle (δ)

The block diagram of controller to compute load angle is shown in Fig. 2. It ensures that the load average power and losses in the VSI are supplied by the source [7]. Alternately, P_{loss} responsible for maintaining dc link voltage must be equal to shunt link power P_{sh}. Comparing P_{loss} and P_{sh}, an error is generated which is passed through a PI controller to compute δas follows:

$$\delta = K_{pa}(P_{loss} - P_{sh}) + K_{ia}\int(P_{loss} - P_{sh})\,dt \quad (9)$$

Where, K_{pa} and K_{ia} are proportional and integral gains of the inner PI controller respectively. The value of shunt link power, P_{sh}, is computed using a MAF as follows:

$$P_{sh} = \frac{1}{T}\int_{t_1}^{t_1+T}(V_{ta}\,i_{fta} + v_{tb}i_{ftb} + v_{tcc}i_{ftc})\,dt \quad (10)$$

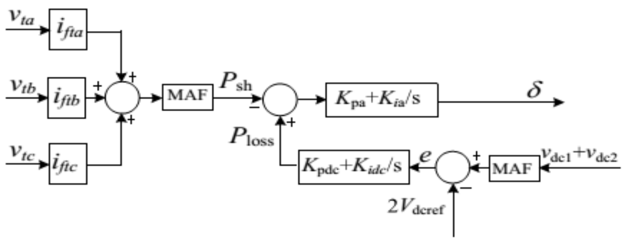

Fig.2. Controller to calculate δ and P_{loss}.

A positive value of P_{sh} means power flow from DSTATCOM to load terminal, whereas negative value of P_{sh} represents power flow from load terminal to DSTATCOM. In steady state, VSI losses are compensated by taking power from the source. Hence, P_{sh} will be negative in steady state. Moreover, capacitor voltage decreases from its reference voltage in steady state. Deviation of capacitor voltage from reference voltage represents losses in the VSI. Hence, P_{loss} will be negative during steady state. Therefore, at all time, P_{sh} and P_{loss} should be equal. Hence, difference of P_{sh} and P_{loss} should be minimized. Output of inner PI controller, shown in Fig. 2, is delta which ensures that shunt link power P_{sh} drawn from source equals to losses in the capacitor P_{loss}.

C. Generation of Instantaneous Reference Voltage

By knowing the zero crossing of phase-a source voltage, selecting suitable reference load voltage magnitude from (8) and computing load angle from (9) the three phase reference voltages are given as follows:

$$v_{trefa} = \sqrt{2}V_t^* \sin(\omega t - \delta)$$
$$v_{trefb} = \sqrt{2}V_t^* \sin(\omega t - \frac{2\pi}{3} - \delta)$$
$$v_{trefc} = \sqrt{2}\,V_t^* \sin(\,\omega t + \frac{2\pi}{3} - \delta\,) \quad (11)$$

Where, ω is the frequency

D. Generation of Switching Pulses

Each phase of the VSI can be controlled independently and hence, a discrete model of single phase has been derived to generate switching pulses. Dynamics of filter inductor and capacitor can be presented by following equations:

$$\frac{dv_{fc}}{dt} = \frac{1}{c_{fc}}i_{fi} - \frac{1}{c_{fc}}i_{ft}$$
$$\frac{di_{fi}}{dt} = -\frac{1}{l_f}v_{fc} - \frac{R_f}{l_{fi}} + \frac{V_{dc}}{l_f}\,u \quad (12)$$

Matrix representation of (12) is given as follows:

$$\dot{x} = Ax + Bz \quad (13)$$

$$A = \begin{bmatrix} 0 & \frac{1}{c_{fc}} \\ -\frac{1}{l_f} & -\frac{R_f}{l_{fi}} \end{bmatrix}, \mathrm{B} = \begin{bmatrix} 0 & -\frac{1}{c_{fc}} \\ \frac{V_{dc}}{l_f} & 0 \end{bmatrix}$$

$$x = [v_{fc}\,i_{fi}].^t\ ,\ \ z = [u\ \ i_{fi}]^{\,t}\ .$$

Where,(13), given in continuous form, can be represented in discrete time form as follows:

$$x(k+1) = Gx(k) + H\,z(k) \quad (14)$$

Where, matrix G and H are given as

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}, \quad \mathrm{H} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}$$

From (14) capacitor voltage will be

$$v_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{fi}(k) + H_{11} u_k + H_{12} i_{ft}(k) \qquad (15)$$

The reference voltage, Vt ref, is maintained at the load terminal. A cost function, J, is chosen as

$$\mathrm{J} = [v_{tref}(k+1) - v_{fc}(k+1)]^2 \qquad (16)$$

Cost function is

$$v_{fc}(k+1) = v_{tref}(k+1) \qquad (17)$$

Finally, reference discrete voltage control law from (15) and (17) is given as

$$u^*(k) = {v_{tref}(k+1) - G_{11} v_{fc}(k) - G_{12} i_{fi}(k) - H_{12} i_{ft}(k)} \Big/ {H_{11}} \qquad (18)$$

$U^*(k)$ is regulated around a hysteresis band h to generate switching pulses of VSI using hysteresis control.

V. MATLAB/SIMULINK RESULTS

Here simulation is carried out in several cases, in that 1) Proposed DSTATCOM Topology for PQ Improvement Features. 2) Proposed DSTATCOM Topology Applied to Induction Machine Drive.

Case 1: Proposed DSTATCOM Topology for PQ Improvement Features

Proposed Novel Multifunctional Distributed Compensation Scheme can mitigate several power quality (PQ) problems. In current control mode (CCM), it injects harmonic and reactive components of load currents to make source currents balanced, sinusoidal, and in phase with load voltages. In voltage control mode (VCM), it regulates load voltage at a constant value to protect sensitive loads from voltage disturbances such as sags, swells, transients, and/or fluctuations. However, the objectives of these two modes are different and it can be Achieve by proposed DSTATCOM.

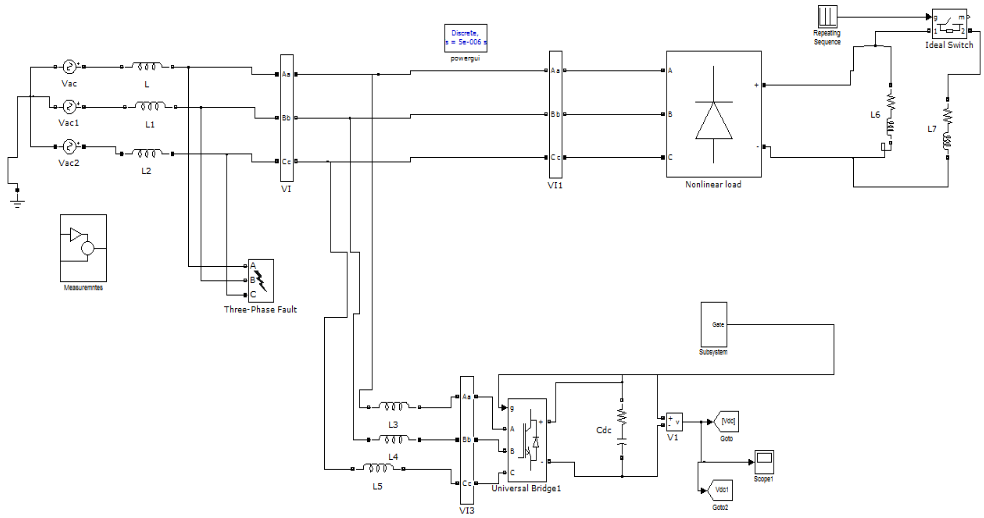

Fig.3 Mat lab/Simulink Model of Proposed DSTATCOM Topology for PQ Improvement Features

Figure.3: gives the Simulation model of system with M-DSTATCOM. In a distribution system with a non-linear load connected to the system will generates harmonics. A nonlinear load in a power system is characterized by the introduction of a switching action and consequently current interruptions. This behavior provides current with different components that are multiples of the fundamental frequency of the system. These components are called harmonics. The amplitude and phase angle of a harmonic is dependent on the circuit and on the load it drives.

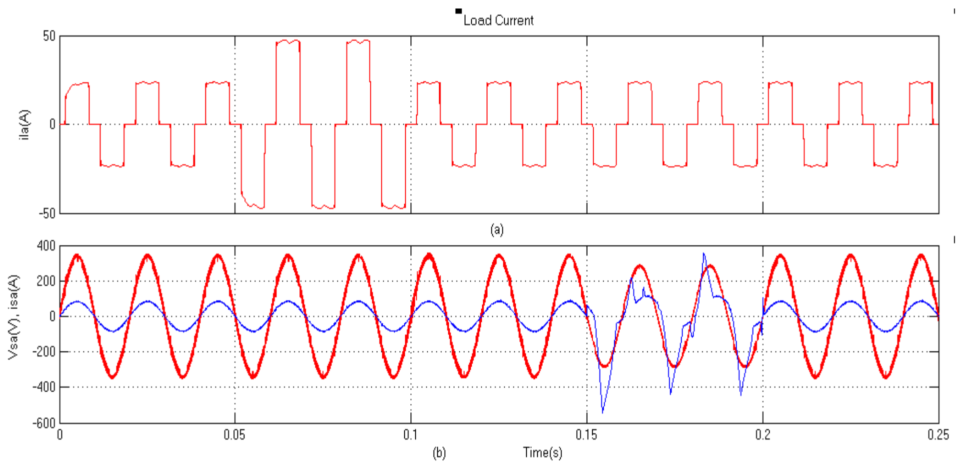

Fig.4 Phase-a wave forms before, during, and after load change. (a) Load current. (b) Source voltage and source current of Proposed DSTATCOM Topology with stiff source.

Initially, a three phase and non-linear load is connected. For achieved multifunctional DSTATCOM operation there phase fault is connected at source side. And at load side an ideal switch breaker is connected. Which is closed at t = 0.05 s. Then load is increased but source currents are balanced and sinusoidal and CCM mode is achieved. It can be seen that both voltage and currents are in phase with each other, maintain unity power factor. Increased load current will not effect on source performance and vice versa. It showed in phase-a, is shown in fig.4 (a).

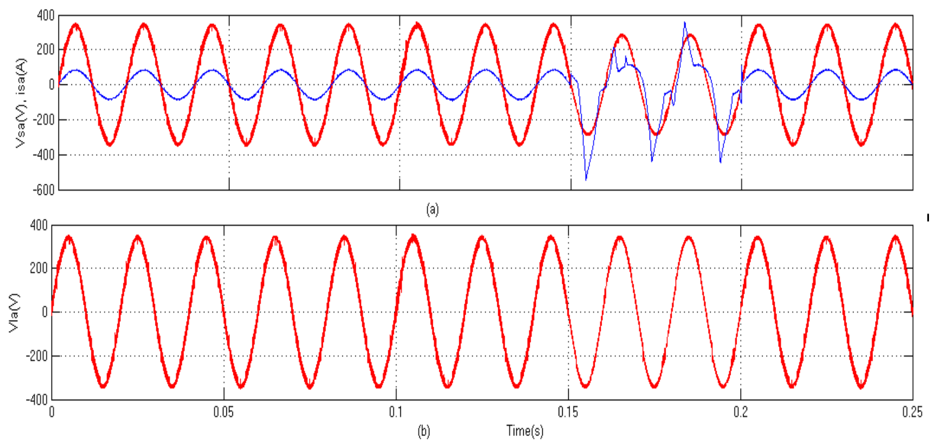

Fig.5: Phase-a: waveforms before, during, and after sag. (a) Source voltage and source current. (b) Load voltage of Proposed DSTATCOM Topology with stiff source.

At t = 0.15 s, fault is created by three phase fault at source side. But a fast voltage regulation is provided at load side. It can be seen in fig. 5, here voltage control mode is performed.

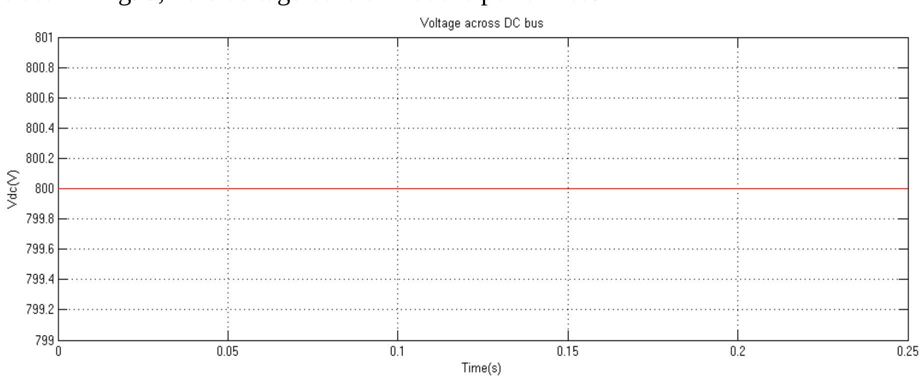

Fig.6 voltage across dc bus

Fig.6: shows the load angle shows the voltage at dc bus which is regulated around 800 V during entire operation.

Case 2: Proposed DSTATCOM Topology Applied to Induction Machine Drive

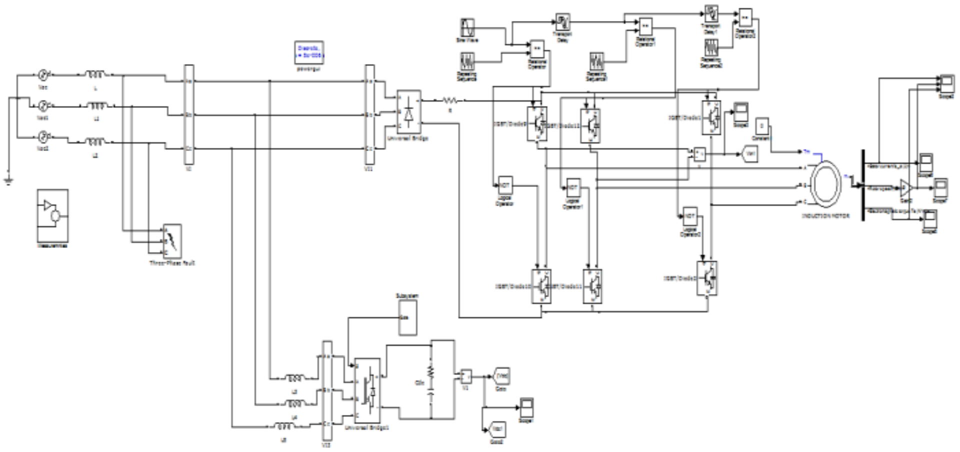

Fig.7Matlab/Simulink Model of Proposed DSTATCOM Topology for PQ Improvement Features with Induction Machine Drive Application

Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Pulse Width Modulation variable speed drives are increasingly applied in many new industrial applications that require superior performance for controlling the power flow for this industrial application requires Facts device, which is operated under distribution system is nothing but distributed compensation scheme.

A DSTATCOM is capable of compensating either bus voltage or line current. If it operates in a voltage control mode, it can make the voltage of the bus to which it is connected a balanced sinusoid, irrespective of the unbalance and distortion in voltage in the supply side or line current. Similarly when operated in a current control mode, it can force the source side currents to become balanced sinusoids.

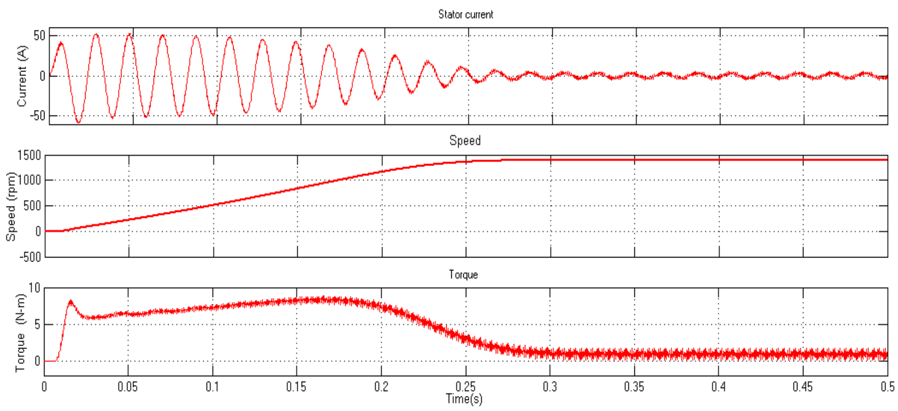

Fig.8: Armature Current, Speed, Electromagnetic Torque

Fig.8: shows the Armature Current, Speed, and Electromagnetic Torque of Proposed DSTATCOM Topology for PQ Improvement Features with Induction Machine Drive Application.

VI. CONCLUSION

In this paper, a new converter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability with a new control algorithm based multifunctional DSTATCOM is proposed to protect the load from voltage disturbances under stiff source. It has been achieved by placing an external series inductance of suitable value between the source and the load. In addition, instantaneous reference voltage is controlled in such a way that the source currents are indirectly controlled and advantages of CCM operation are achieved while operating in VCM for permissible range of source voltage. Moreover protects the Induction machine drive through DSTATCOM under power quality concerns with near to optimal features with efficient operation.

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