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An FPGA based Area-Delay Efficient 64-bit Carry Select Adder Design for High-Speed Applications

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Abstract:- In present scenario of VLSI based system designing, efficient area, low power and high speed are the main parameter of design research. The designs must have the desired functionality and also parametric optimized performance. System portability, faster time to market and cost efficiency are the non-technical parameters that effect the life-time performance of the designed system. The low power consumption of VLSI circuit has emerged as the most important design parameter as it directly or indirectly affects the performance of all other technical and non-technical system design parameters. In the present work a Carry-Select-Adder (CSA or CSLA) design with low power combinational design is presented. The design is synthesized and simulated on Field Programmable Gate Array based VLSI hardware for its functional and power performance. The present study presents a comparative speed and power analysis of the proposed work with some existing work. The FPGA based low power analysis is concluded on the basis of the proposed work. The present work is performed using Xilinx Tool.

Keywords:- Carry Select Adder, Half Sum Generator, Half Carry Generator, Carry Select Unit, Dynamic Power.

I. INTRODUCTION

In the VLSI based system design the main areas of research in present scenario are the low power, reduced size and high speed path logic systems. Since most of the processing are based on the very basic operation of binary addition, the requirement of high speed addition and multiplication is always needed for achieving the desired performance of high speed processors. In the digital system, the speed of addition operation depends on the propagation of carry in the sequential behaviour in the adder circuit. The carry propagates sequentially from single-bit addition logic to the next-bit addition logic and upto the last bit addition. So, this causes a large delay in the adder circuits. The carry propagation operation becomes the main limitation of any adder bit design. The delay parameter becomes more critical in the adders with a larger length of data. This delay is reflected in the complete processing system as the data has to be synchronized throughout the system units that are operating parallel. Many designers and researchers have worked to propose various adder architectures to optimize the carry propagation delay. Many types of adder architectures are available such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Skip Adder, Carry Save Adder and Carry Select Adder. These adders have their own architectures with their own advantages & disadvantages. The present work shows implementation of a 64-bit Carry Select Adder design. The present study shows the power and frequency based analysis of the carry select adder design and a comparison between previously proposed design performances with the present design performance. The different sections of the proposed work are arranged as follows: Section II presents a concise literature survey of the related work and its applications. Section III describes the architecture of 64-bit carry select adder design and the building blocks of the design. Section IV presents the simulation and synthesis results of the work performed in this paper. Section V presents the conclusion based on the present work. And in the last all the references are mentioned.

II. LITERATURE REVIEW

High performance VLSI systems are increasingly required in the development of modern instruments, devices, gadgets and systems. An Adder is very important performance deciding hardware unit of the VLSI systems that require high speed processing. An efficient design of Adder essentially improves the performance of complex systems. A number of modifications are proposed by researchers to suggest improvements in the performance of carry select adder. A new logic formulation for CSLA is proposed in [1,2]. In this paper all the redundant logic operations present in the conventional CSLA are removed. This paper proposes a scheme where carry select (CS) operation is scheduled before the calculation of the final SUM. A review on the performance of various architectures of carry select adder for their speed and area is presented in [3]. Reference [4] proposed area-efficient carry select adder that have low power consumption. This paper work uses the concept of sharing the common Boolean terms to reduce the duplicate adder cells. This work used 1-XOR Gate and 1-inverter for

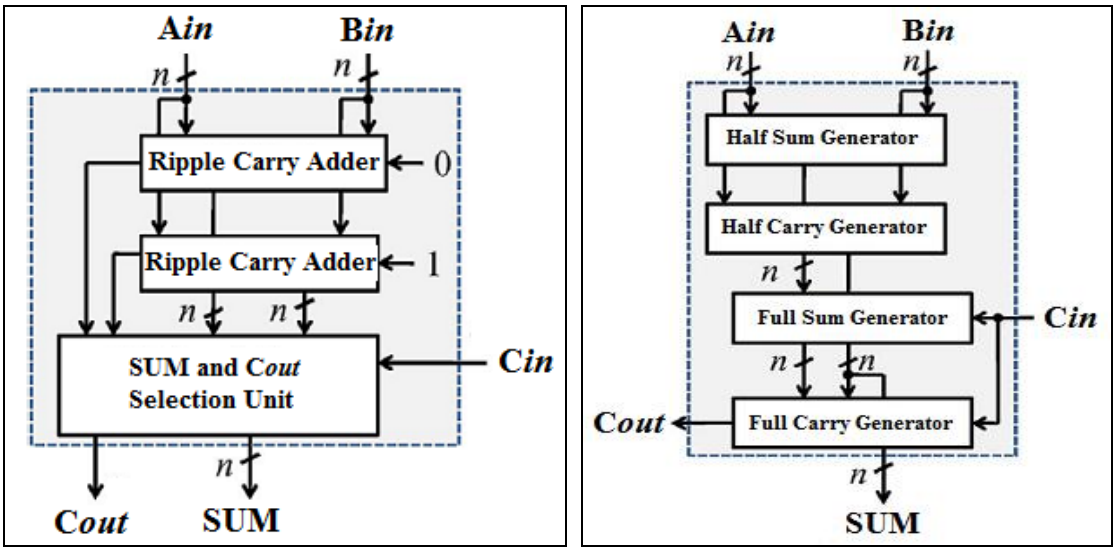
each summation operation and, 1-AND Gate and 1-OR gate in each carry-out operation. An optimized delay and area based design of 16-bit, 32-bit and 64-bit CSLA adder is proposed and compared with the conventional design in [5, 6]. Reference [7] presents an analysis of conventional CSLA and Binary to Excess-1 Converter (BEC) CSLA. This reference presents an innovative 16-bit CSLA architecture that replaced the BEC using D-latch.

A simple and efficient gate-level modification in the architecture of carry-select-adder is proposed in [8] to show a significant reduction in the area and the power of the conventional CSLA design. This paper replaced the ripple-carry-adder in the conventional architecture, with Cin='1, with BEC to achieve low area and power performance. A redundant logic optimized modified design is simulated in [9, 10, 11, 12, 13] to propose an area-delay-power reduced architecture of CSLA with respect to the conventional CSLA architecture. A modified CSLA is designed and proposed in [14] that can add upto five 16-bit numbers with the help of compressors by following the procedure of basic carry select adder. This work shows a higher efficiency in the speed operation of addition of multiple numbers.

A gate level modification in the conventional CSLA in proposed in [15] to show a sophisticated and area-power efficient CSLA architecture. Minimized logic operation based architecture is used in this referenced paper to improve the efficiency of the conventional CSLA. A 16-bit Square-Root CSLA (SQRT-CSLA) architecture and a modified SQRT-CSLA are presented and simulated in [16] to evaluate the performance of the presented designs. This paper concluded an area efficient architecture of the SQRT-CSLA. An analysis of performance comparison between conventional CSLA and SQRT-CSLA are presented in [17]. In [18] a comparative analysis of conventional CSLA, BEC-based CSLA, CBL-based CSLA and Area-Delay-Power efficient CSLA is presented. The architectures of CSLA are analyzed for multiple length addition operations and application of CSLA in ALU architecture is presented. A new CSA design technique is proposed in [19] that does not use multiplexer. This architecture is designed with 16-bit, 32-bit and 64-bit lengths and the results are compared with the conventional architectures for analyzing the efficiency of the proposed design. In [20] a modified architecture of CSLA is used that uses a Logical Converter Unit (LCU) to work similarly as BEC to efficiently optimize the area-delay-power parameter with respect to the conventional designs. This work is performed on the gate level architecture modification over the conventional architecture of the CSLA. A gate-level modified architecture over the conventional CSLA is proposed in [21] to optimize the power-delay product based performance of the adder architecture.

III. ARCHITECTURE OF CARRY SELECT ADDER

All The architecture of the conventional carry select adder has two types of basic units: (1) ripple carry adder (RCA) unit, and (2) sum and carry selection (SCG) unit. The ripple carry adder caused the delay in the addition operation. The delay is a function of the length of the adder. The logic block diagram of the conventional carry select adder is shown in Fig 1(A). In this architecture, there are two 'n'-bit ripple carry adder blocks with *Ain* and *Bin* are inputs to these adders. The two RCA units has different carry inputs, one with *logic-'0'* carry input and the other with *logic-'1'* carry input. The outputs of the RCA units are the inputs of the sum and carry selection unit. The SCG unit selects the output based on the value of the carry *Cin* input of the adder. The basic architecture of the sum and carry selection unit is a multiplexer with the *Cin* input acting as the selection control input of the multiplexer. The logic block diagram of an 'n'-bit ripple carry adder unit is shown in Fig 1(B). It has four logic blocks: (1) half sum generator (HSG) unit, (2) half carry generator (HCG) unit, (3) full sum generator (FSG) unit, and (4) full carry generator (FCG) unit. The inputs to the HSG and HCG units are the adder inputs *Ain* and *Bin*. Whereas the inputs of the FSG and FCG units are the outputs of the HSG and HCG units and the adder carry input *Cin*. The outputs of the ripple carry adder units are a function of the carry input to the adder. As clear from the logic diagram, the carry input to both the RCA block in the conventional CSA are fixed logic values. Thus, RCA blocks are used to generate the sum and the carry outputs of the adder with respect to the pre considered logic-'0' and logic-'1' input carry values. These outputs are selected on the basis of the actual logic value of the carry *Cin* input of the adder.



(A) **(B)**

Fig.1: Logic Block Diagram of: (A) Conventional Carry Selector Unit, and (B) Ripple Carry Adder

The architecture of an 'n'-bit modified CSA design is shown in Fig 2. The modified architecture has five blocks to perform the addition operation: (1) half sum generator (HSG) unit, (2) carry generator with '0' input (CG0), (3) carry generator with '1' input (CG1), (4) carry select unit (CS or CSU), and (5) full sum generator (FSG). The modification in the architecture is performed in the carry evaluation stage of the adder as compared to the conventional design. In this architecture, the carry is generated at the first stage of processing for two fixed initial carry values, i.e., logic-'0' and logic-'1' carry values. The output of these blocks is used to select the final carry on the basis of the carry *Cin* input of the adder. The carry bits generated from CS unit are used in the FSG to generate the sum output. Table I specifies the logic gates that are used to realize the gate level architecture of the internal blocks of the CSA.

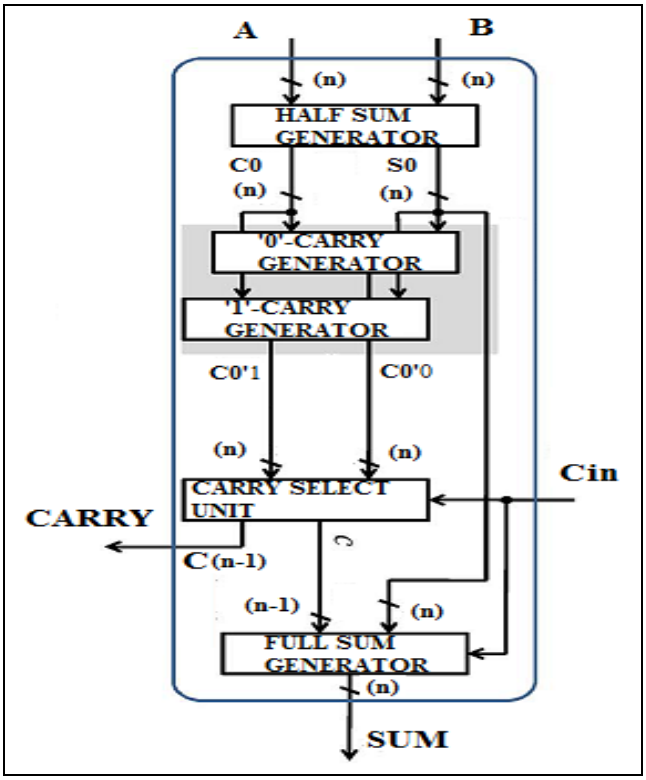


Fig.2: Logic Block Flow Diagram of Carry Select Adder

Table I: Logic Gates used for CSA Block Realization

CSA Block	AND Gate	OR Gate	XOR Gate
HSG	✓	x	✓
CG0	✓	✓	x
CG1	✓	✓	x
CSU	✓	✓	x
FSG	x	x	✓

IV. SIMULATION AND SYNTHESIS RESULTS

In The design is simulated for functional performance and power consumption. The power consumption analysis is performed using Xilinx XPower Tool. Fig 3 represents the graph of Dynamic Power variation of the proposed design with respect to the variation in the operational clock frequency on Kintex-7 device. The graph shows a linear variation in the dynamic power with respect to the clock frequency. Table II presents the comparison of the result from the work performed and the previous proposed design results. The comparison concludes an efficient reduction in the operational delay of the circuit performance in this work. The Power-Delay product proves the efficiency of the design realization on the configurable FPGA device of Xilinx from Kintex-7 Family. The FPGA that is used to perform simulation and synthesis of the present work is XC7K70T-2LFBG676. The simulation of the design is performed on Xilinx ISim Tool using VHDL Test-Bench. The RTL schematic block diagram of the proposed design is shown in Fig. 4. The result of functional simulation is shown in Fig 5.

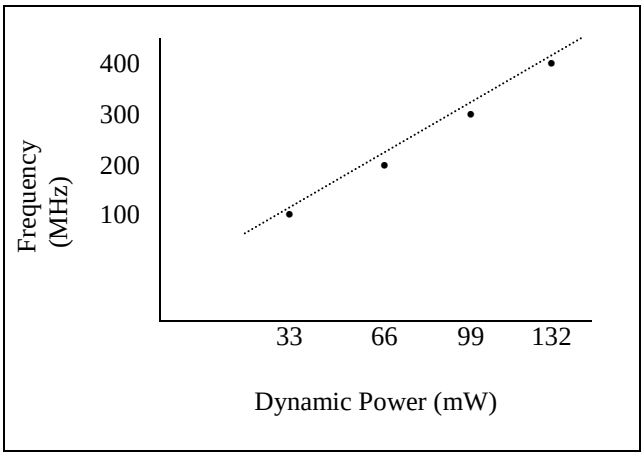


Fig.3: Frequency Versus Dynamic Power variation of proposed design for Kintex-7 Family FPGA Device

Table I: Power-Delay Product Performance based Comparison of Proposed Design with Existing Designs

Carry Select Adder	Power (mW)	Delay (ns)	Power-Delay Product
64-bit Proposed Design	27 (100MHz)	16.032	433
	81 (300MHz)		1299
	134 (500MHz)		2148
64-bit Conventional CLA [10]	97	28.281	2743
64-bit CLA Proposed Design [10]	72	25.209	1821
16-bit CSLA ADP Efficient Design [18]	229	10.192	2334
16-bit CSLA Proposed [18]	221	9.894	2187

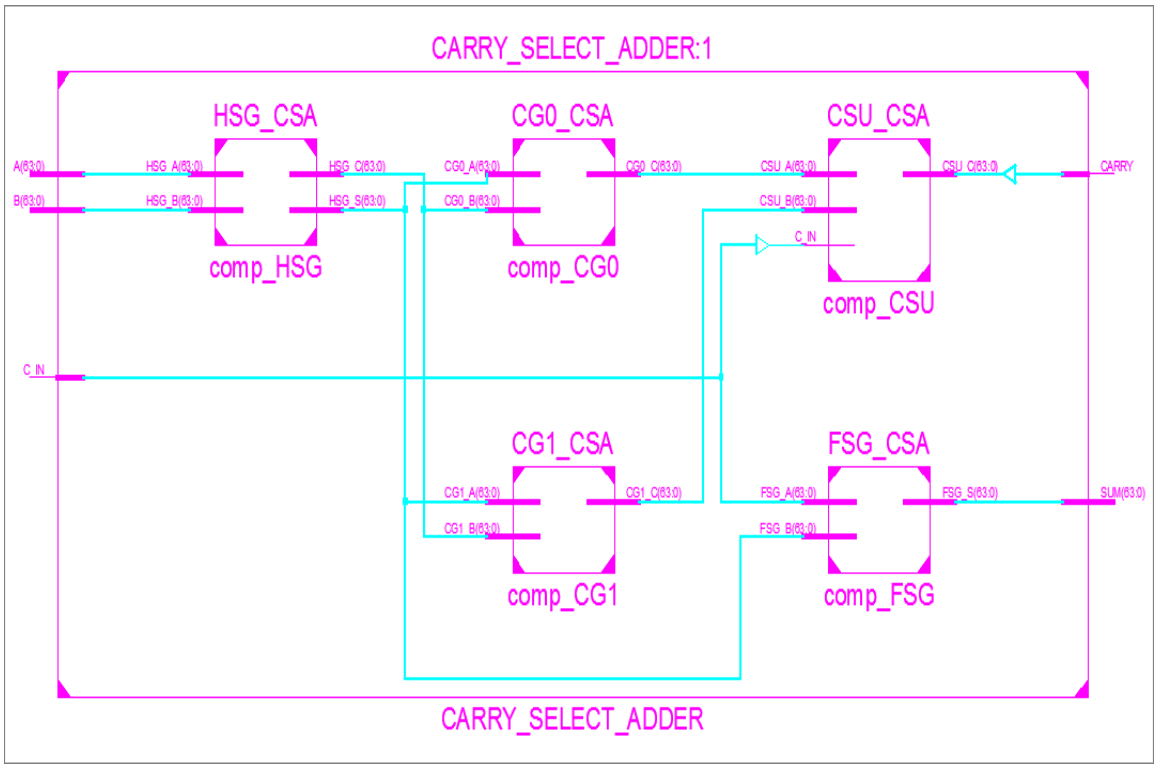


Fig.4: RTL Schematic of Carry Select Adder

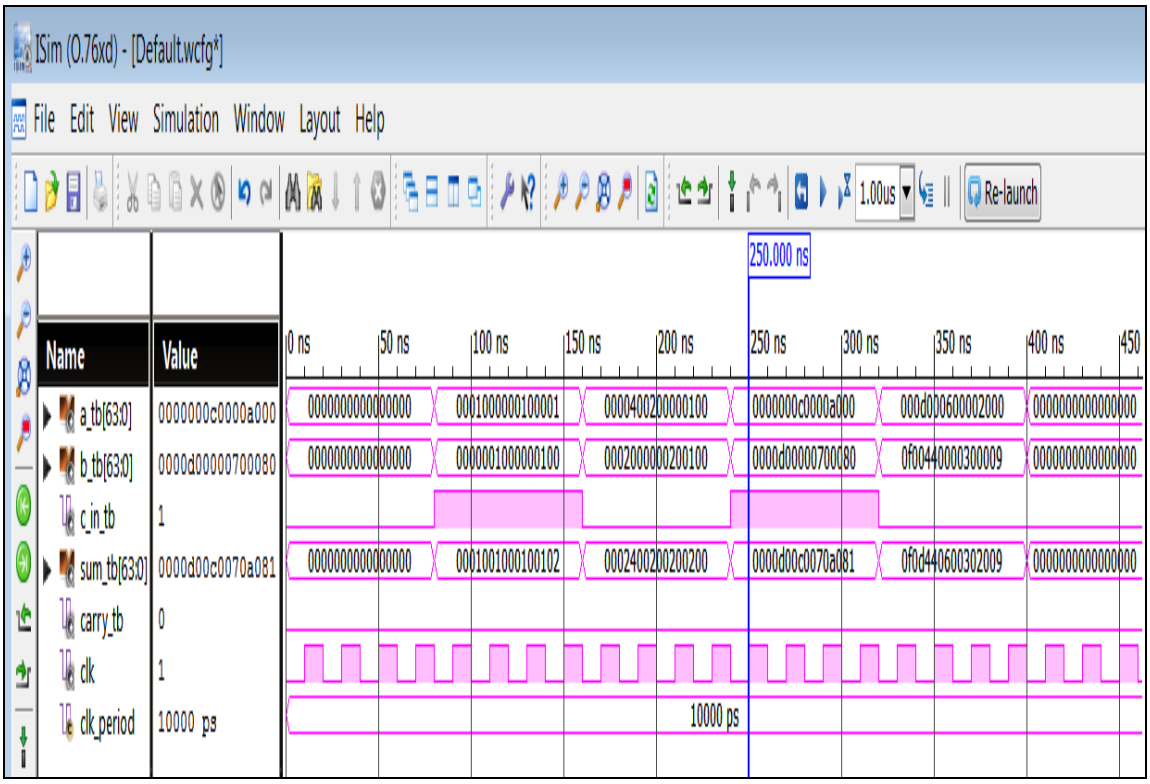


Fig.5: Waveform Simulation of Carry Select Adder

V. CONCLUSIONS

In the present work a 64-bit design of carry select adder is simulated for frequency versus power performance on different programmable devices. The analysis has shown the comparative power consumption by the devices. The Kintex-7 family FPGA has shown comparative minimum power consumption for implementing the proposed design in application circuits. The present work based analysis also indicates that

low power implementation hardware can be used for applications with a FPGA that has low internal voltage (V*int*) and low auxiliary voltage (V*aux*). The present design uses a combinational design for addition of 64-bit binary numbers. This design can be used with signal processing applications that require addition operation hardware. In future the multiplier and the test pattern generator can be configured to match the application specific requirement of the design for a BIST based hardware design implementation. The present work also has the scope of combining other existing hardware designs with this design for a complex logic implementation.

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