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Digital Implementation of Costas Loop with Carrier Recovery

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Abstract:- Demodulator circuit is a basic building block of wireless communication. Digital implementation of demodulator is attracting more attention for the significant advantages of digital systems than analog systems. The carrier signal extraction is the main problem in synchronous demodulation in design of demodulator based on Software Defined Radio. When transmitter or receiver in motion, it is difficult for demodulator to generate carrier signal same in frequency and phase as transmitter carrier signal due to Doppler shift and Doppler rate. Here the digital implementation of Costas loop for QPSK demodulation in continuous mode is discussed with carrier recovery using phase locked loop.

Keywords:- Software Defined Radio, Doppler Shift, Doppler Rate, Phase Locked Loop

I. INTRODUCTION

The function of demodulator is to demodulate the received signal from wired or wireless link which can be coherent or non coherent. Generally coherent demodulation technique is used because of its several advantages [1]. For coherent demodulation signal with same frequency and phase as transmitted signal is required at receiver side. But as signal propagates from transmitter to receiver, there is a change in amplitude, frequency and phase of the received signal. It is very difficult for receiver to generate coherent signal for demodulation. Carrier frequency offset recovery and Bit synchronization is important task of coherent demodulator.

In wireless communication there is always a shift in phase and frequency of received signal. For example satellite communication or in GPS it introduce Doppler shift in frequency [5]. So, different errors like constant phase error, constant frequency offset and changes in frequency with time which is Doppler rate need to be corrected. Doppler rate can be characterized as a frequency ramp input. Phase Locked Loop is heart of design of demodulator. The loop filter in PLL is responsible for correcting this phase and frequency errors. Second order loop filter presented here which is able to correct constant phase and frequency offset [2], [3]. For Doppler rate tracking third order loop filter is adopted [5]. Gain margin, Phase margin, loop gain, noise bandwidth and stability are important parameters for third order loop filter design [5].

Digital Signal Processing is the fastest growing segment of the communication industry. If we take example of traditional wireless device, it only works on a single standard. Also it is expensive to upgrade as standard is changing rapidly as technology changes. It is possible to reduce amount of hardware and analog signal processing with the collection of hardware and software technologies called Software Defined radio [2]. SDR makes system flexible. SDR is emerging as an important commercial technology due to rapid deployment to market.

II. DIGITAL COSTAS LOOP ARCHITECTURE

Received signal is passed from band pass filter centered at IF frequency and bandwidth is chosen 1.5 times signal bandwidth [4]. Band Pass Filter is analog filter used as anti aliasing filter in order to filter out of band component. After filtering, continuous time signal is converted into discrete time signal using sampler. Here sampling rate is chosen according to nyquist criteria.

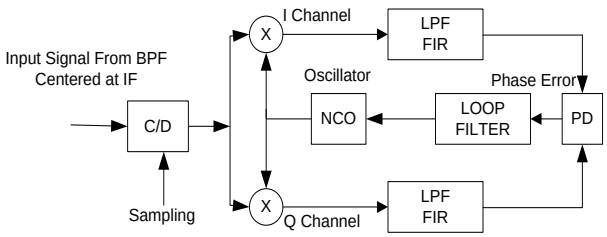

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Fig. 1: Digital Costas Loop Architecture

For IF to baseband conversion, signal with frequency and phase synchronism with transmitted carrier signal must be required. Here Numerically Controlled Oscillator generates two signals,

$$I(t) = \cos(\omega_c t + \varphi)$$
$$Q(t) = \sin(\omega_c t + \varphi)$$

Where φ is the phase difference between the local carrier signals generated by Numerically Controlled Oscillator and input modulated signal. From above mixing of two signal yields, ω_c is the carrier frequency of transmitted signal.

$$S_I(t) = m(t)\cos(\omega_c t) \times \cos(\omega_c t + \varphi)$$
$$S_I(t) = \left(\frac{1}{2}\right) m(t)[\cos(\omega_c t) + \cos(2\omega_c t + \varphi)]$$

And,

$$S_Q(t) = m(t)\cos(\omega_c t) \times \sin(\omega_c t + \varphi)$$
$$S_Q(t) = \left(\frac{1}{2}\right) m(t)[\cos(\omega_c t) + \sin(2\omega_c t + \varphi)]$$

Low pass filter eliminate high frequency component from above two signals which yields,

$$S_I(t) = m(t)\cos(\omega_c t)$$
$$S_Q(t) = m(t)\sin(\omega_c t)$$

Taking arc tangent of two phase error difference

$$\varphi(t) = \tan^{-1}\left(\frac{S_Q(t)}{S_I(t)}\right)$$

This phase error is filtered by loop filter which is used to drive Numerically Controlled Oscillator. Oscillator adjusts the phase and frequency until signal tracks on sent carrier frequency.

III. DIGITAL IMPLEMENTATION OF SUB MODULES

a. IF to Baseband Conversion

Band pass sampling method is adopted for conversion of continuous time signal into discrete time signal [6]. If carrier frequency is high, baseband sampling method requires high speed Analog to Digital Converter which results in high power consumption. For example we want to sample signal with 70MHz carrier frequency and 384 KHz bandwidth. According to sampling theorem minimum 140 MHz sampling rate is required which is twice of carrier frequency. Such high rate is not necessary. Band pass sampling requires sampling rate twice of signal bandwidth. In above case minimum band pass sampling rate is 768 KHz. This will shift IF in within f_s /2. This down converted IF is generated at local oscillator for baseband conversion. Sampling of analog signal and down conversion can be done in single step with the help of band pass sampling.

b. Arm filter or Low Pass Filter

The function of low pass filter is to remove $2\omega_c$ component from mixer outputs. For better performance, two low pass filters with identical performance for I and Q channel is required [2]. However it is not possible with the analog low pass filters. With the help of digital implementation low pass filters with identical performance can be implemented. Finite impulse response filter are used because of its linear phase characteristics [3]. If order of low pass filter is high, performance would be better but it consumes more hardware resource [2]. Pass band and stop band frequencies and attenuation should be selected according to performance tradeoffs.

c. Phase Locked Loop

Phase Locked Loop is a key component in carrier and timing recovery. Phase detector, Loop filter and numerically Controlled Oscillator are elements of phase locked loop. Among all three parts, design of loop filter has major impact on performance of the PLL. Importance of loop filter is to generate a useful error while suppressing the effect of the noise as much as possible [8]. The order and the noise bandwidth determine the performance of the loop filter [5], [8].

1) ***Phase Detector:*** Phase detector is important component of Costas phase locked loop. For All digital Phase locked, various phase detectors like PFD (phase frequency detector), EX –OR gate, Flip flop can be used [3]. However for achieving better phase estimation, CORDIC based phase detector is used in digital implementation [2]. In conventional Costas loop phase detector, true value of phase difference is approximated by sine of phase difference. Hence error is large. Also lot of hardware recourse is used if multiplier phase detector is implemented on FPGA [3]. So, shift and addition based Coordinated Rotation Digital Computer algorithm is used as a phase detector. Arc tangent phase detector is widely used due to its high precision. it is shown that the arctangent phase detecting method is the only method which could keep

linear in the half (+ 90 °) interval of input error range [3]. Here the output is the phase difference, not approximation, so the precision of phase detecting is higher. Here CORDIC algorithm is shown below.

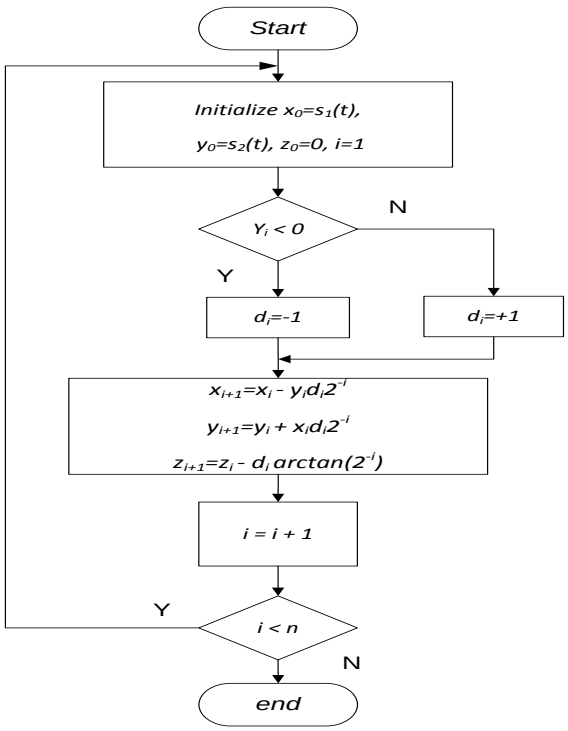

Fig. 2: CORDIC Algorithm

Here pipelined architecture is used. It needs three adders, two shift registers and one coefficient memory. This architecture can save many resources. It is suitable for software defined radio in receiver.

2) Loop Filter: The order and bandwidth are the important parameters of the loop filter design. Under the low signal to noise ratio, performance of demodulator depends on the loop parameters. There is trade off in the loop design. Desired loop SNR depends upon the loop bandwidth [8]. Here the first order active loop [filter for second order phase locked loop is shown below.

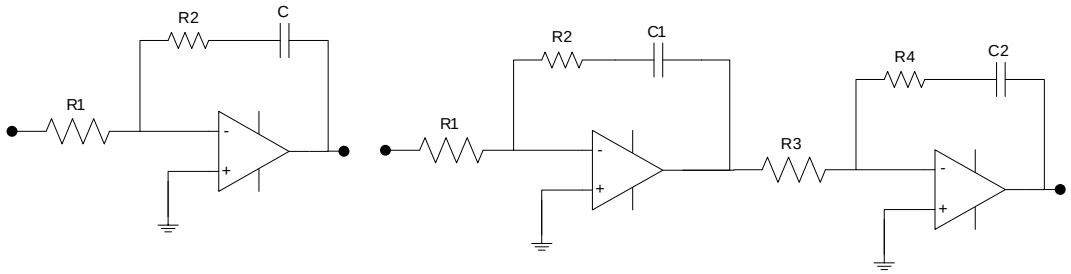

Fig. 3: First order PI loop filter and Second Order Gardner filter

The loop bandwidth is selected as shown below. The phase error variance $\sigma\emptyset^2$ within the loop is given by,

$$\sigma\emptyset^2 = \frac{1}{\rho_L S_L}$$

Where, ρL is Loop SNR required for satisfactory performance. Minimum 6dB SNR is required. The squaring loss S_L in the QPSK system is approximately given by [4],

$$S_L = \frac{1}{\left[1 + \frac{4.5}{SNR_i} + \frac{6}{SNR_i^2} + \frac{1.5}{SNR_i^3}\right]}$$

Phase error variance $\sigma\emptyset^2$ within is also given by,

$$\sigma\emptyset^2 = \frac{B_L}{W_L} * \frac{1}{SNR_i}$$

Where, SNR_i is Signal to Noise Ratio at the input of demodulator, W_L is Arm Filter bandwidth in Costas loop, B_L is Loop bandwidth required. Input signal to noise ratio at the input to the demodulator which is given by

$$\mathrm{SNR_i} = \frac{\mathrm{E_b}}{\mathrm{N_0}} * \frac{\mathrm{R_b}}{\mathrm{B_i}}$$

Where, E_b/N_0 is Bit signal to Noise Ratio, R_b is Data rate (bits/sec) and B_i is IF filter Bandwidth of filter at input of demodulator. Natural frequency ω_n can be found out after selecting proper damping ratioξ. For Butterworth filter, choose ξ as 0.707. Relation between loop bandwidth, natural frequency and damping ratio is given by,

$$\mathrm{B_L} = \frac{\omega_n}{2}\left(\xi + \frac{1}{4\xi}\right)$$

Loop filter constant τ_1 and τ_2 can be found from below equation

$$\omega_n = \sqrt{\frac{K_0 K_d}{\tau_1}} \quad \text{and} \quad \xi = \frac{\omega_n \tau_2}{2}$$

Where K_0 and K_d are Phase detector and Voltage are controlled oscillator gain. The lock range $\Delta\omega_L$ should be less than overall loop gain [1],

$$\Delta\omega_L \leq K_0 K_d$$

Loop filter transfer function is given by,

$$F(s) = \frac{1 + s\tau_2}{s\tau_1}$$

To convert s domain transfer function into Z domain Bilinear Transform is used.

$$S = \left(\frac{2}{T}\right)\frac{1 - Z^{-1}}{1 + Z^{-1}}$$

Here T is given as sampling time, direct form II or I realization of loop filter in z domain is used for digital implementation. Consider the open loop transfer function for a third order phase locked loop with Gardner's filter [5],

$$F(s) = \frac{(s\tau_2 + 1)^2}{(s\tau_1)^2}$$

Open loop transfer function,

$$H_{OL} = \frac{\sqrt{2P}\, K_0 K_d}{s}\frac{(s\tau_2 + 1)^2}{(s\tau_1)^2}$$

To perform bode analysis of this third order loop,

$$20Log|H_o\ (j\omega)| = 20Log\left[\frac{\sqrt{2P}\, K_0 K_d}{{\tau_1}^2}\right] + 40Log|1 + j\omega\tau_2| - 60Log|j\omega|$$

$$\angle\, H_o\ (j\omega) = 2\, tan^{-1}[\omega\tau_2] - 270^o$$

Because of the three perfect integrators in the open loop transfer function order N=3. There are two repeated zeros corresponding to ($s\tau_2$+1), and no poles other than the perfect integrators. Here it is shown that open loop phase is a function of only parameter τ_2, this provide our design concept. Low value of phase margin tends the loop towards instability, and also unnecessarily increases the noise bandwidth.

$$\tau_2 = \frac{1}{\omega_0} tan\left[\frac{90^o + Phase\ Margin}{2}\right]$$

From value of τ_2, we can calculate value of

$$\tau_1 = \sqrt{\frac{\sqrt{2P}\, K_0 K_d}{\omega_0^3}}(1 + \omega_0^2 \tau_2^2)$$

Here ω_0 is Unity gain frequency.

3) Numerically Controlled Oscillator: Numerically controlled oscillator is used instead of voltage controlled oscillator. The goal of NCO is to produce two local orthogonal carrier signals. The direct frequency synthesizer technology is adopted for that purpose [7].

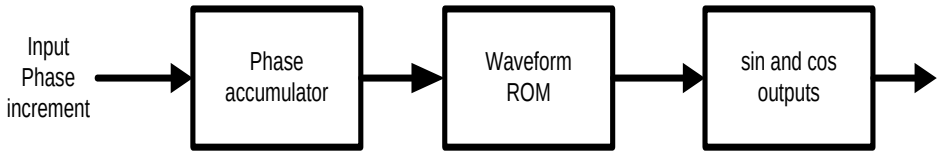

Fig. 4: Numerically Controlled Oscillator

NCO consist of two parts, phase accumulator and ROM waveform tables. Orthogonal signals are generated using method of lookup table. The output frequency is defined asf_0 [7],

$$f_0 = \frac{\Delta\theta\ f_s}{2\pi\ 2^N}$$

Where f_s is sampling frequency, N is phase accumulator word size and $\Delta\theta$ is phase increment. Here is the output of the phase detector, which is filtered by loop filter and gives discrete phase increment value. Phase increment value $\Delta\theta[n]$ is given by,

$$\Delta\theta[n] = 2\pi\ 2^N \left(\frac{f_c}{f_s} + e[n]\right)$$

Where, f_c is the center frequency. The output of the phase accumulator $\theta[n]$ is given by after phase wrapping

$$\theta[n] = \sum_{i=0}^{n} \Delta\theta[i]\ \ (mod\ 2\pi\ 2^N)$$

Output of the NCO is written as,

$$NCO\ \cos[n] = cos\left(\frac{\theta[n]}{2^N}\right)$$

$$NCO\ \sin[n] = sin\left(\frac{\theta[n]}{2^N}\right)$$

So, after putting phase accumulator output in above equations, output of numerically controlled oscillator is given by,

$$NCO\ \cos[n] = cos\left(2\pi\left[n\left(\frac{f_c}{f_s}\right) + \sum_{i=0}^{n} e[i]\right]\right)$$

$$NCO\ \sin[n] = sin\left(2\pi\left[n\left(\frac{f_c}{f_s}\right) + \sum_{i=0}^{n} e[i]\right]\right)$$

This sine and cosine waves are used for coherent demodulation of input signals.

IV. CONCLUSION

Second order and third order phase locked loop for carrier recovery in Doppler environment can be designed in analog domain and converted into digital domain using bilinear transform. Digital demodulator can be designed and verified using MATLAB/Simulink and it can be realized on FPGA. Digital implementation of demodulator reduces many problems associated with analog implementation. Advantages include superiority in performance, speed, reliability and reduction in size.

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