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Single Hard Fault Detection in Linear Analog Circuits Based On Simulation before Testing Approach

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Abstract:- A method for single hard fault detection in linear analog circuits based on simulation before testing approach is proposed in this paper. Simulation before testing approach locates or identifies faulty components of the circuit under test (CUT) by creating a fault dictionary for all the potentially faulty components from the simulation of CUT. In the proposed approach, the CUT is simulated using Modified Nodal Analysis (MNA) to find the values of circuit parameters or diagnosis variables. Test vectors corresponding to the components of CUT are generated from the circuit matrix which act as key feature in identifying the potentially faulty components and are treated as fault dictionary. Test vectors are used to determine the diagnosis variables for testing. The tolerance problems of analog circuit testing as well as the sensitivity of the test vectors to component values affect the practical possibility of the approach. To solve this, test vectors are generated for upper and lower bound values of the components of CUT and testing is performed. A CUT is said to be fault free if the circuit variables are within the fault free range. Fault variables corresponding to the components of CUT are derived and the fault variable which has lowest relative standard deviation is found and the corresponding component is declared as faulty. The proposed approach is tested on bench mark circuits and validated through the results obtained from simulation.

Keywords:- linear analog circuits – modified nodal analysis- test vector – fault diagnosis- hard faults

I. INTRODUCTION

Analog circuit testing is an important research problem due to non availability of standardized methods or procedures. The factors like tolerance and nonlinearity of circuit components limit development of standard methods for single or multiple faults in analog circuits. Analog circuit faults are modeled as parametric or soft faults and catastrophic or hard faults. Parametric or soft faults are hard to detect as they cause degradation in system performance where as hard faults cause topological changes and complete system performance variation. Fault detection methods are classified as simulation before testing (SBT) and simulation after testing. Simulation before testing approach is based on the development of fault dictionary which consists of the details regarding the variation in diagnosis variables for different faulty conditions of the components of CUT which requires larger data base. Simulation after testing approach performs simulation on the obtained diagnosis variables measurements to identify the faulty components which requires high computational cost. Most of the research proposals are for parametric faults detection as they are difficult to find. But it becomes necessary to locate hard faults to isolate as well correct them. In [1], circle equation-based modeling method suitable for locating parametric and hard faults is being proposed. The equation is independent from the value of element to be modeled, and uniquely determined by its location and the nominal values of the remaining elements in the circuit under test. Hence, the circle equation can model any continuous parameter shifting or hard fault occurs. Three points are sufficient to determine a circle; therefore, only three simulations corresponding to three distinct faulty parameters are used to model all parameter shifting faults. In [2], a wavelet based method is proposed to locate parametric and hard faults in analog circuits. In wavelet analysis of diagnosis variables, two test metrics, one based on a discrimination factor using normalized Euclidean distances and the other utilizing Mahalanobis distances, are introduced and they rely on wavelet energy computation. Tolerance limit, the factor that affects fault detectability, for CUT is set by statistical processing data obtained from a set of fault-free circuits. A fault dictionary based method based on weighted Mahalanobis distance based on the entropy theory is proposed in [3] and this method can reduce the fuzzy groups of analog circuits to some extent, and it is suitable for not only soft fault diagnosis, but also hard fault detection. A new fault modeling method applicable for both hard and soft faults is proposed in [4]. This approach models faults based on a function which is independent of the values of components of CUT and to resolve the tolerance effect minimum distance approach is used. A complex field modeling approach which is applicable for both hard and soft faults is proposed in [5] and is based on frequency selection method. Test vector based approach is used in [6] to locate single parametric faults. The proposed

approach uses the test vector as in [6] but aims to locate hard faults in linear analog circuits and also provides solution to solve the tolerance challenge in analog circuit testing and also the sensitivity of the test vector to components values.

Section 2 of this paper explains the mathematical fundamentals of the proposed approach. Section 3 deals with the detailed test procedure or flow and section 4 discusses the simulation results obtained on the bench mark circuit. Section 5 concludes.

II. MATHEMATICAL FUNDAMENTALS

Analog circuit testing begins with the simulation of CUT to derive the diagnosis variables such as node voltages and branch currents. Simulation involves formulation of the circuit equation and solving it for the unknowns. To simulate the CUT, Modified Nodal Analysis (MNA) is used. It handles voltage sources effectively by an unknown current through it and adds it to the vector containing unknown node voltages. MNA for linear systems results in the system equation of the form

$$AX = Z \tag{1}$$

where A is the coefficient matrix or the circuit matrix which is formed by conductance of the components of CUT and the interconnections of the voltage sources. X is the unknown vector consists of circuit variables (node voltages and few branch currents) which are useful for testing and Z is the excitation matrix. The right hand side matrix (Z) consists of the values of independent current and voltage sources.

$$X = \begin{bmatrix} V_n \\ I_v \end{bmatrix} \tag{2}$$

$$Z = \begin{bmatrix} I \\ V \end{bmatrix} \tag{3}$$

Faults in the CUT are simulated using Fault Rubber Stamp (FRS) as explained in [6-8]. FRS is based on the MNA stamp of the components of a CUT. The MNA stamp of a component C_n connected in between the nodes j and j' (V_j , V_j'- respective node voltages) ,in the coefficient matrix is,

$$\begin{array}{c} \\ j \\ j' \end{array} \begin{array}{c} \begin{array}{cc} V_j & V_{j'} \end{array} \\ \begin{bmatrix} +C_n & -C_n \\ -C_n & +C_n \end{bmatrix} \end{array} \tag{4}$$

If this component is assumed to be faulty, its value changes from C_n to $C_n \pm \Delta$. This deviation causes the current through that faulty component to deviate from its nominal value. This current deviation called fault variable (ϕ) is introduced in the faulty circuit unknown matrix as an unknown branch current. To indicate the current deviation through the faulty component, the faulty component is represented as a parallel combination of its nominal value and the deviation (Δ) (fig.1). V_j and V_j' are the node voltages at the nodes j and j' respectively. i_f is the current deviation through the faulty component.

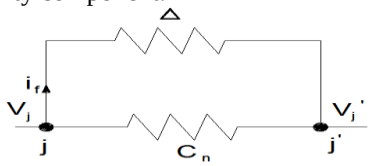

Fig.1 Faulty Component representation

The fault rubber stamp for the component C_n is,

$$\begin{array}{c} \\ j \\ j' \\ \\ f \end{array} \begin{array}{c} \begin{array}{cccc} V_j & V_{j'} & & i_f \end{array} \\ \left[\begin{array}{ccc|c} +C_n & -C_n & \vdots & 1 \\ -C_n & +C_n & \vdots & -1 \\ \cdots & \cdots & \cdots & \cdots \\ \hline 1 & -1 & \vdots & -\Delta^{-1} \end{array}\right] \end{array} \tag{5}$$

The bottom row line is the faulty component equation and the right most column corresponds to the extra fault variable. As seen in (6), for each faulty component there is an additional column at the right side and row at the bottom of the coefficient matrix is introduced. The faulty system with the FRS in matrix form is,

$$\begin{bmatrix} A & c \\ r & \Delta \end{bmatrix} \begin{bmatrix} X_f \\ \phi \end{bmatrix} = \begin{bmatrix} Z \\ 0 \end{bmatrix} \tag{6}$$

where c and r are the additional column and row introduced corresponding to a faulty component. The additional column c indicates the location of the faulty component. The additional row r is the faulty component equation with its node voltages. The value of Δ depends the faulty value of the component. It can be observed that a new variable called fault variable (ϕ) is also introduced as unknown into the unknown vector matrix (X_f) of the faulty circuit. It can also be noted that this fault variable is the unknown branch current. As seen in (7), the coefficient matrix (A) of the nominal circuit is retained in forming the faulty system equation without any modification in the values of it. Thus from (7), the faulty circuit equations are written as,

$$AX_f + c\phi = Z \tag{7}$$

$$rX_f + \Delta\phi = 0 \tag{8}$$

replacing $Z = AX$ from (1),

$$AX_f + c\phi = AX \tag{9}$$

$$A(X - X_f) = c\phi \tag{10}$$

$$X - X_f = A^{-1}c\phi \tag{11}$$

$$X - X_f = T\phi \tag{12}$$

$$\phi = (X - X_f)/T \tag{13}$$

$$T = A^{-1}c \tag{14}$$

The product $A^{-1}c$ is a complex column vector and it is called test vector [6]. As c describes the location of a component in the CUT, the test vector is associated to that component and the values are independent of the faults. Thus the fault variable which can be obtained by the element wise division of the difference vector (difference between the nominal and the faulty solutions) and the test vector is also associated to a specific component in the CUT. It is observed that the test vectors are sensitive to the component values and they carry the information regarding the location of the components. In real time, the fault free components may be within the tolerance limits (not exactly the nominal value). The fault detectability is affected if testing is performed with the test vectors simulated with nominal values. To solve this, this paper generates test vectors for lower and upper bound values of components to test the circuit.

III. TEST PROCEDURE

Test procedure consists of two phases namely pre testing and testing stages. In the first phase called pretesting stage, test vectors are generated for upper and lower limits of components values. These test vectors can be treated as fault dictionary. The circuit variables or the diagnosis variables are obtained by solving the MNA equations with the nominal, upper and lower bound circuit component values and stored. The CUT is said to be fault free only when the circuit variables measured at the test nodes are within the bound values. In the second stage called test stage, faults are injected into the CUT and measurements are made at the selected nodes.

The fault variable is found from (14) with upper and lower bound test vectors. The average and relative standard deviation related to the average of each column (associated with the components in CUT) of fault variable matrix is found. An element of the CUT is said to be faulty when the estimated relative standard deviation is the lowest value. The detailed flow is shown in fig. 2 & 3.

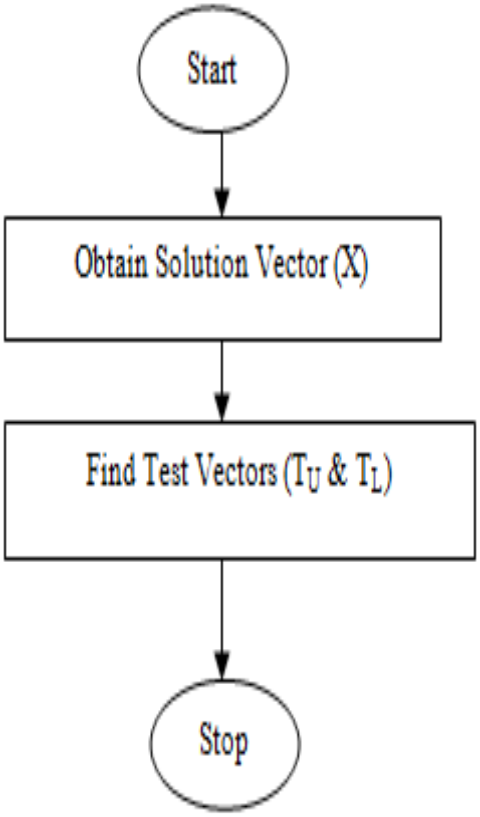

Fig. 2: Pre testing stage

IV. SIMULATION RESULTS

Simulation results on the linear voltage divider (LVD) show the efficiency of the proposed approach. Test vectors are generated for the lower and upper bound values of components and are shown in figure 5 &figure 6. All the components are assumed to have 5% tolerance and the circuit is shown with nominal values in figure 4. Two diagnosis variables measured at the output (node 6 voltage) and input (node 1 current) are used for testing. These variables are selected as they are input and output nodes which are easily accessible for measurement and also the test vectors corresponding to these variables are found to have different value. The fault detectability is affected by the diagnosis variables for which the test vectors are same. The same value test vectors lead to same fault variable, so the faults cannot be distinguished.

Hard faults on passive components of CUT are simulated by assuming 1Ω for short circuit faults and $2\times10^{9}\Omega$ for hard faults. Single hard faults are injected into the CUT and the diagnosis variables are measured. The fault variables are obtained by measuring the diagnosis variables for the upper and lower bound values of components of CUT (except for faulty component). The average and relative standard deviation relative to the average value are estimated and found to be the lowest value for the faulty component. For example, the short circuit of R_1 leads to a fault variable of 8.85E-16 where as for other components of CUT the values are found to be 0.95, 2.27, 2.69, 2.8, 0.7, 1.75, 2.6, 2.76, 2.81. From this it can be observed that the relative standard deviation is the lowest value for R_1. Hence R_1 is faulty. For other fault types the values are shown in table 1.

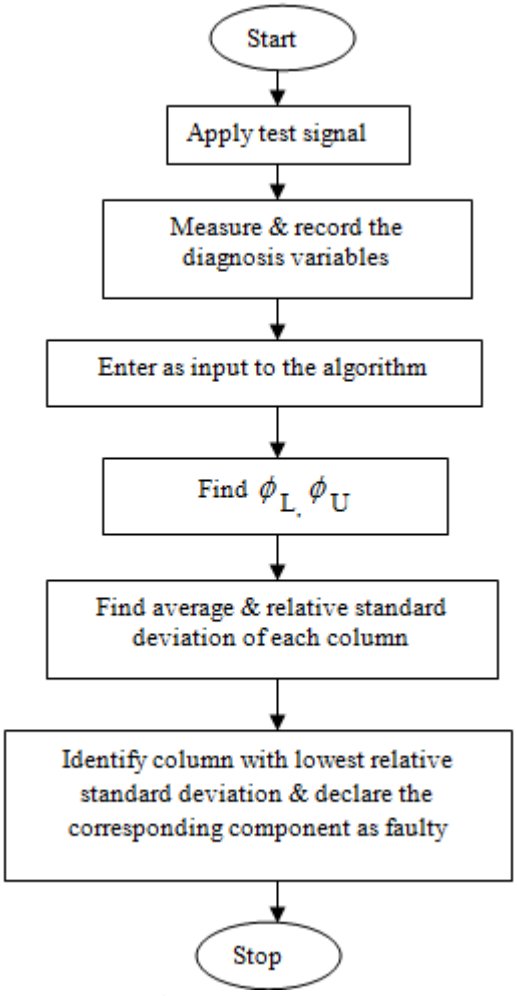

Fig. 3: Testing Stage

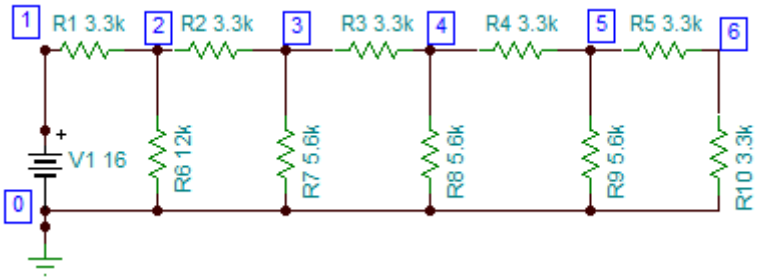

Fig. 4: Linear Voltage Divider

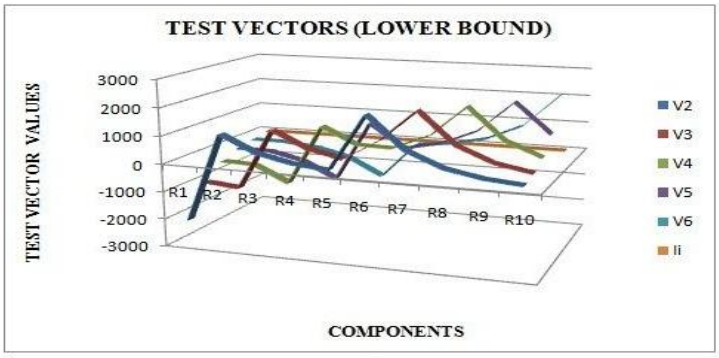

Fig.5: LVD lower bound test vectors

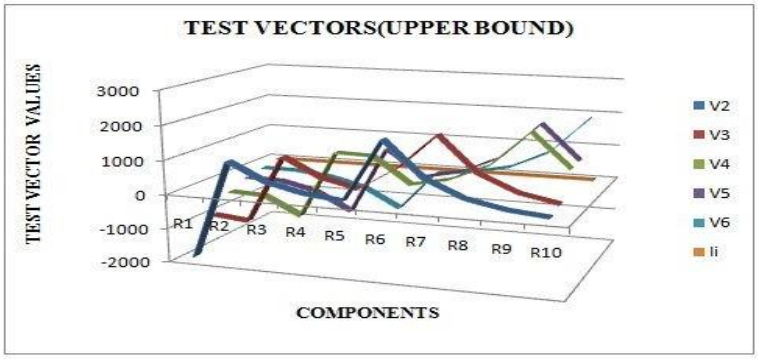

Fig. 6: LVD lower bound test vectors

Table 1: Results of Linear Voltage Divider

Fault Type	Relative Standard Deviation of fault variables corresponding to components of CUT										Lowest Value of Relative Std. Deviation
	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	
R_1 Short	8.85E-16	0.95	2.27	2.69	2.8	0.7	1.75	2.6	2.76	2.81	8.85E-16
R_2 Short	0.95	1.2 E-15	1.8	2.5	2.8	1.04	1.01	2.3	2.7	2.8	1.2 E-15
R_3 Short	2.3	1.8	6.45 E-16	1.8	2.6	2.3	1.02	1.01	2.3	2.7	6.45E-16
R_4 Short	2.7	2.6	1.8	1.48E-14	1.8	2.7	2.3	1.03	1.01	1.6	1.48E-14
R_8 Short	2.5	2.3	1.01	1.03	2.3	2.6	1.8	5 E-15	0.9	2.2	5E-15
R_9 Short	2.8	2.7	2.3	0.95	1.1	2.8	2.6	1.8	3.5 E-15	1.7	3.5E-15
R_{10} Short	2.8	2.79	2.7	2.3	0.9	2.75	2.8	2.5	1.7	3.9 E-15	3.9E-15
R_3 Open	2.3	1.8	5.05E-15	1.8	2.6	2.3	1.02	1.01	1.6	2.5	5.05E-15
R_4 Open	2.7	2.6	1.8	8.31 E-15	1.8	2.7	2.3	1.02	1.01	1.6	8.31E-15
R_5 Open	2.8	2.76	2.56	1.8	3.9 E-14	2.81	2.7	2.3	1.7	0.9	3.9E-14
R_6 Open	0.08	1.02	2.3	2.7	2.8	2.5 E-15	1.8	2.6	2.8	2.81	2.5E-15
R_7 Open	1.8	1.01	1.02	2.3	2.7	1.8	6.4 E-15	1.8	2.6	2.76	6.4E-15

V. CONCLUSIONS

A simulation before test approach to locate single hard faults in linear analog circuits based on test vector is proposed. The CUT is simulated using modified nodal analysis and test vectors corresponding to all components of CUT are derived and are stored as fault dictionary. Suitable diagnosis variables for testing can be identified or selected from the test vectors and it is sufficient to store only those test vectors. And it is also possible to identify the components that can be detected under faulty conditions (testable group) by finding the same value test vectors. To solve the problem of tolerance in real time testing, test vectors are generated for upper and lower bound values of components of CUT. Simulation results displayed show the efficiency of the proposed approach.

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