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Symmetrical Multilevel Inverter with Reduced Number of switches With Level Doubling Network

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Abstract:- A multilevel inverter is a power electronic device that is used for high voltage and high power application because of its characteristics of synthesizing a sinusoidal voltage on several DC levels. They give good quality output resulting with lower harmonic distortion in the output. This paper proposes a new topology of a multilevel inverter that utilizes less number of switches in the circuit. The objective of this new topology is to increase number of levels with a lower number of switches and sources without adding any complexity to the power circuit. The advantage is to reduce the total harmonic distortion of the inverter output. Here switching patterns are realized using both pulse generation unit and PWM technique and the total harmonic distortion is measured using both the two methods. In this paper multi-carrier pulse width modulation technique are proposed, which can minimize the total harmonic distortion. A modified multilevel inverter topology is also proposed using a level doubling network to the proposed topology. This is realized by adding an extra half-bridge that maintains half the voltage of other full bridges. Also, it generates almost double the number of output voltage levels. The modified topology of multilevel inverter is realized using pulse generator unit and its effect on the harmonic spectrum also analysed. The simulation of proposed and modified topology of multilevel inverter is done by MATLAB/Simulink software.

Keywords:- Proposed Multilevel Inverter, Modified Multilevel Inverter, Level Doubling Network (LDN), Multicarrier PWM Technology (PWM), Pulse Generation Unit

I. INTRODUCTION

Drive is used to transfer power from one side to other. Such transfer of power is obtained by proper switching. Importance of drives is increasing day by day. The main requirement of electric drives are variable voltage, variable frequency source. Inverter is one of the most widely used power electronics device in the world today. The application of inverters can be found in three main categories; power supply, motor drives and active filters. Among the many types of inverters, the multilevel inverter is fast emerging as a popular choice in many industrial applications, from oil and gas, power plant to power quality devices. The staircase output waveform produced by multilevel inverter helps to reduce lower level harmonics while increasing power quality.

Multilevel inverters include diode clamped converter, flying capacitors, cascaded and H-bridge MLI. This MLI help to achieve near sinusoidal output waveforms with reduced THD. As the number of output levels increases, harmonics decreases. The disadvantage of conventional MLI is that if more number of output levels are required, then more number of components are needed and due to this complexity increases in gate driver circuits. At present the most famous hardware implementable topologies are cascaded H-bridge. The drawback of symmetric MLI can be overcome by asymmetric MLI. In this paper a novel symmetric MLI topology is proposed which requires minimum number of switches with reduced THD.

II. SYMMETRICAL MULTILEVEL INVERTER

A. Proposed Multilevel Inverter

Conventional cascaded multilevel inverters require large number of switches and these power switches are combined to generate an output in positive and negative polarities. This topology requires less switches.

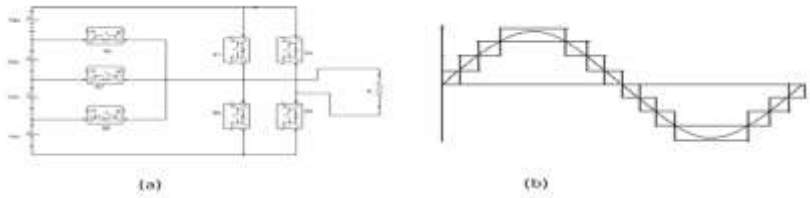
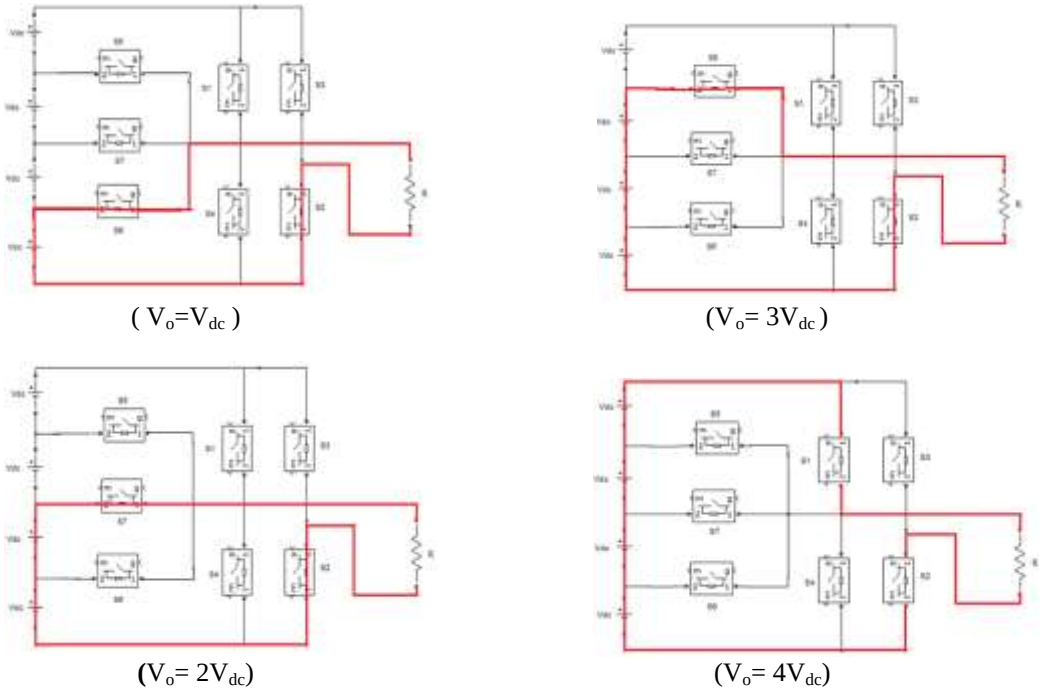


Fig. 1: (a) Basic multilevel inverter block (b) 9-level Output Waveform

The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to its own dc source Vdc. By cascading the ac outputs of each H bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, each H-bridge inverter can produce nine different voltages levels. The main aim of introducing the proposed cascaded multilevel inverter is to increase the number of output voltage levels by using minimum number of power electronic devices. The proposed basic unit is comprised of four dc voltage sources, and seven switches.



($V_o=V_{dc}$) ($V_o= 3V_{dc}$)

($V_o= 2V_{dc}$) ($V_o= 4V_{dc}$)

Fig.2: Modes of Opeartion

Negative voltages are generated by switching other pair of switches S3 and S4. Operation is similar to the above mode shown in Fig. 2. Proposed Multilevel Inverter is working by operating two switches at a time.

III. PROPOSED MLI WITH LDN

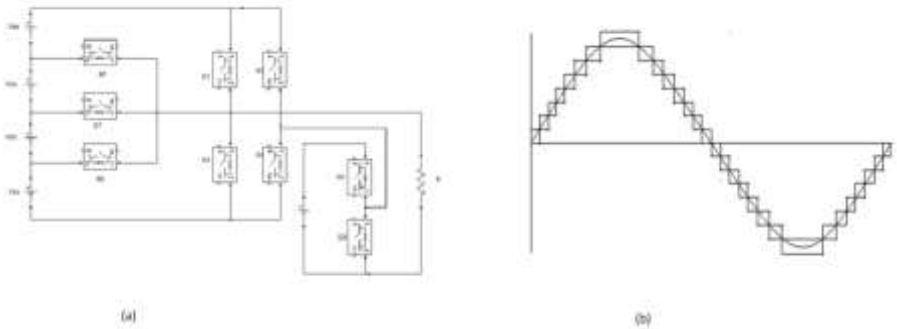


Fig. 3: (a) Basic multilevel inverter block with LDN (b) 17-level Output Waveform

The LDN takes the form of a half-bridge inverter in order to generate almost double the number of output voltage levels. The topology is realized by adding an extra half bridge connected that maintains half the voltage of other bridges by a self-balancing mechanism. N number of H-bridges that are cascaded, then the MLI circuit can generate (2N + 1) levels of output voltage without the LDN. When the half-bridge comes in operation, we get N additional levels in the positive half cycle. Similarly, on the other half cycle, N additional levels are obtained, the symmetry restricts the maximum voltage levels in both positive and negative sides to be 2N, resulting in a total of (4N + 1) levels by including the LDN. If the LDN is added to a (2N + 1) level MLI, the topology will effectively behave like an MLI of (4N + 1) levels, where N is an integer and its value is the number of basic module or number of dc source in the basic module. It gives almost double the number of levels in an MLI, by adding only two switches per phase.
By the introduction of level doubling network, number of levels are increased twice. For this modified MLI only three switches are operated at a time.

IV. CONTROL STRATEGY

The Sinusoidal Pulse Width Modulation (SPWM) is a well known wave shaping technique in power electronics for realization, a high frequency triangular carrier signal V_{car}, is compared with a sinusoidal reference signal V_{ref}, of the desired frequency. The crossover points are used to determine the switching instants. The magnitude ratio of the reference signal (V_{ref},) to that of triangular signal (V_{car}) is known as the modulation index.

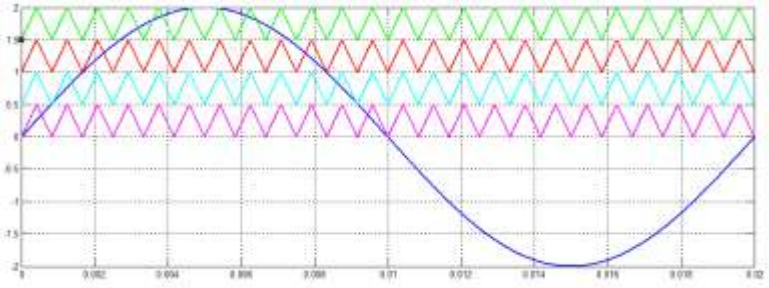


Fig.4 : Multicarrier PWM Strategy

Pulse width modulation is obtained by comparing sinusoidal modulating signal of 50Hz and four carrier signal of each 1.2KHz and equal amplitude.

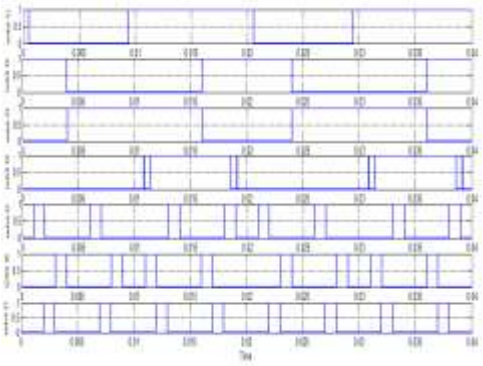


Fig .5 : Pulses for Proposed MLI

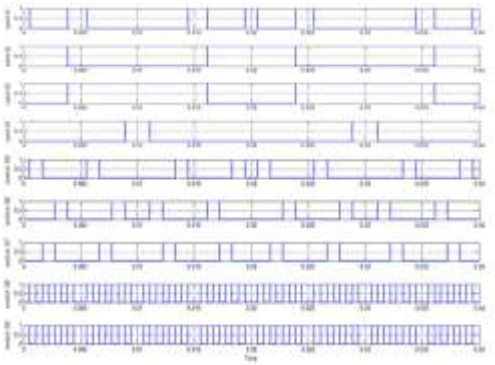


Fig.6 : Pulses for MLI with LDN

These switching patterns are generated by the pulse generation unit by using logic gates AND, OR, and NOT with the total time period of 20msec or 50Hz.

V. SIMULATION RESULT

7-level and 17-level inverter is controlled by multi carrier sinusoidal PWM and using pulse generator block respectively. Pulses block subsytem generates pulses for all the switching devices. DC side has voltage sources, each of 12V. Total Harmonic Distortion block given in the circuit measures the THD for output voltage and output current.

B. **Simulation of Proposed Circuit**

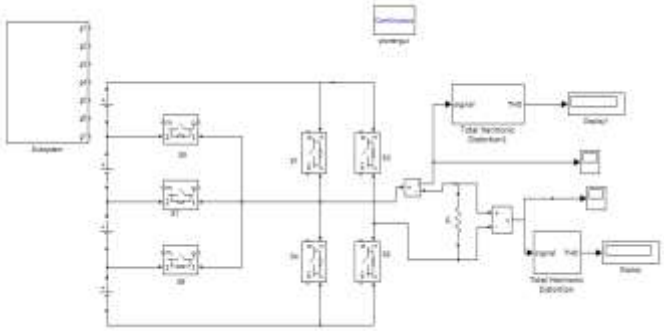
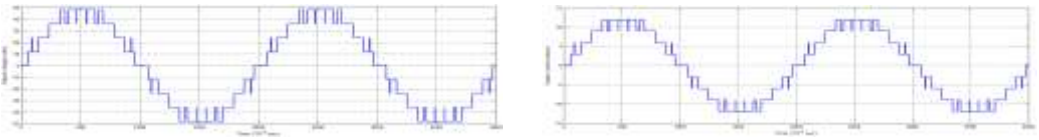


Fig. 7: Simulink model of proposed MLI

Table. I: Simulation Parameters

Simulation Parameters	Values
DC voltage, V_{dc}	12V
Output frequency, F_s	50Hz
Time period , T = 1/Fs	20msec
Carrier signal amplitude, A_c	0.5 units
Carrier frequency, f_c	1.2KHz
Modulating signal amplitude, A_m	2 units
Modulating frequency, f_m	50Hz
Load resistance, R	4 ohms

Output of proposed MLI contains 9 level with 20msec time period or 50Hz frequency with separate DC input each of 12volts and the resistive load of 4ohms. And its THD value of 7-level inverter output voltage is 31.64% and for the output current is 31.62%.



(a) (b)

Fig.10 : Simulation Result of Proposed MLI (a) output voltage (b) output current

C. **Simulation Of Proposed MLI With LDN**

17-levels of output is obtained by cascading LDN to the proposed MLI topology. By this cascaded connection 9 level output can be modified to 17-levels. Control signals for the 9 switches are generated by using pulse generation unit. Both 17-level output voltage and current are in phase because of the resistive load. Output frequency is 50Hz or time period of 20msec. %THD of 17-level inverter output voltage is 19.90% and for the output current is 19.93%.

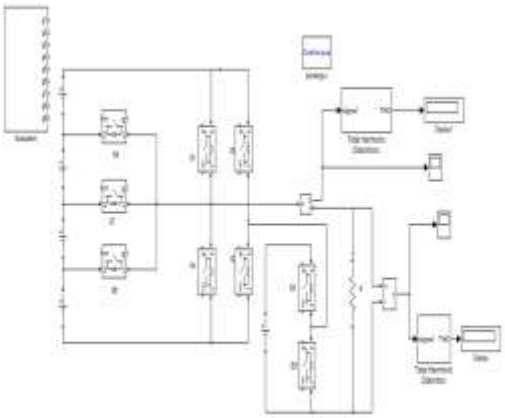


Fig.11 : Simulink Model of MLI with LDN

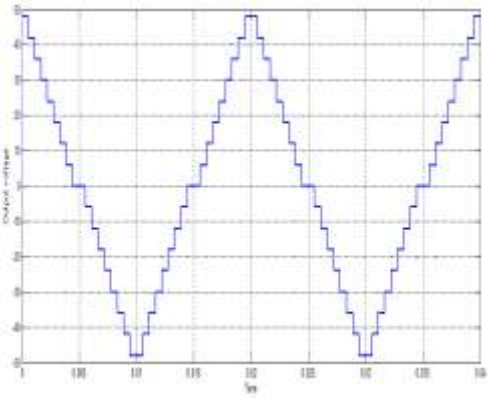


Fig. 12 : Simulation Result of MLI with LDN

VI. CONCLUSIONS

The multilevel inverters can _nd potential applications in adjustable speed drives, where multilevel inverters can solve harmonic problems and also avoid possible high-frequency switching dv/dt induced motor failures. Instead of using cascaded inverter topology, proposed topology is more convenient for all applications because it has less complex control method, give less THD. The proposed inverter topology has the least number of switches compared to other existing conventional topologies. These will allow a higher level with lower THD

values. So this cascaded multilevel inverter to be built using a small number of components; therefore overcome the need for high number of switching devices in a cascaded multilevel inverter design consequently reduce the installation cost and inverter size. The proposed cascaded multilevel inverter topology operation and performance is verified by the simulation in MATLAB 2010a. Hence proposed topology is more convenient than conventional cascaded inverter.

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