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Power And Area Optimization of Pulse Latch Shift Register

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Abstract: - This paper discusses the CMOS layout design of power and area optimized pulse latch shift register. This latch is design with transmission gate. The number of transistors requires for design of latch is less using transmission gates. The decrease in number of transistors' and size shrinking at 50 nm technology will reduce the design area. The transmission gate also reduces the number of stray capacitances will improve speed and power dissipation of design. The shift registers are design using edge triggered flip flops but the use of latches for shift register design also optimizes the area. For this design a non overlap clock pulses are used. This solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

Key words:- Pulse latch, Shift Register, CMOS design,

I. INTRODUCTION

The shift registers are commonly used for memory designs. The shift registers are design using edge triggered flip flops. All the flip flops are synchronized through clock signals. The increase in word length of shift register will increase the number of flip flops. The edge triggered flip flops are design with two or more than two latches. The general structure of flip flop is design using master slave latches. The internal structure of shift register composed of N number of series connected D flip flops. The latches are design using combination multiplexer logic cell using transmission gates. The structure of N bit shift register is composed of series connected synchronized N number of flip flops. The shift register is design with cascaded flip flops hence there is no interconnected circuits between the flip flops hence speed is not the major constraints of shift register design as compare to area and power. The latches are mostly not used in design of shift register ue to its timing problems. The non overlap pulse latches are the better option of design of shift registers. It reduces the number of transistors for design which in turn also reduces the area and power consumption.

II. PULSE CLOCK GENERATOR

In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees. The pulse clock generator generates clock pulses for the level triggering of latch. The pulse clock generates consist of two bit counter and 2X4 decoding circuit. The two bit counters output is connected to the two inputs of decoder circuit. The output of decoder generates logic high pulses at its anyone output at one time. These outputs are the connected to the level trigger clock signal of pulse shift register. The schematic design of pulse clock generator is shown in fig 3. The counter is design with flip flops using master slave arrangement of two latches. The decoder circuit is design using four AND logic gates and two NOT logic gates. This design requires 10 transmission gates out of which two transmission gates are connected to the reset signal of counter circuit. The same reset signal is further use to reset the pulse shift register circuit. The schematic design of clock pulse generator consist of 17 NOT logic gates and 4 AND gate requires total 78 MOS transistors.

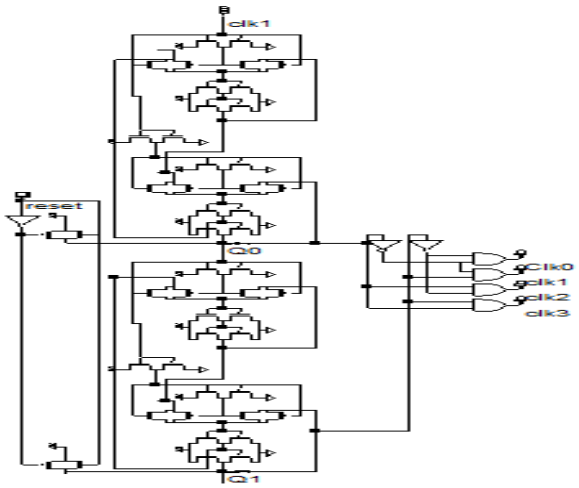

Figure1: Schematic Diagram for pulse clock generator

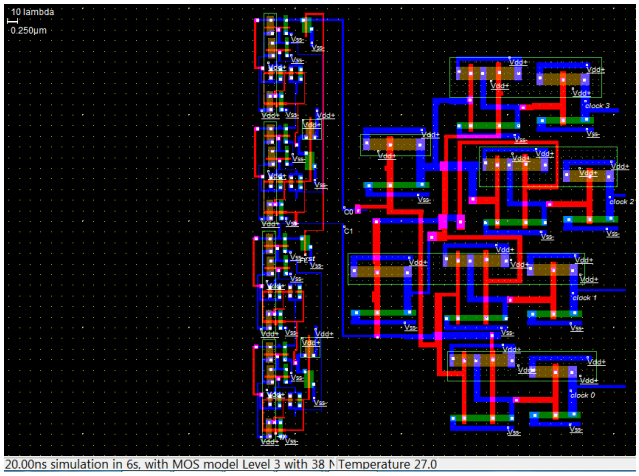

Figure2: CMOSLayout Design for clock pulse generator

Fig 2 shows the CMOS layout design for clock pulse generator. The design is composed of two bit counter and a 2:4 decoder circuit. The decoder circuit generates the four clock pulses of finite time duration which can be further use for pulse clock signals of shift registers latches.

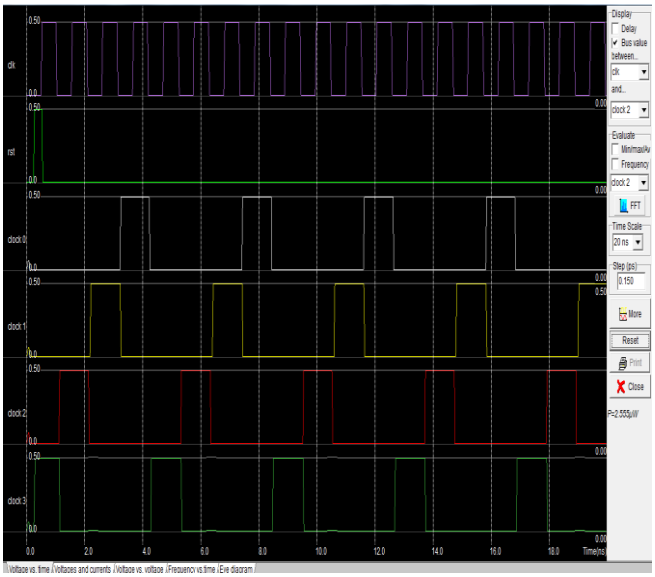

Figure3: Timing Simulation for clock pulse generator

Fig 3 shows the timing simulation of clock pulse generator. For each edge triggered clock the pulses of finite duration are generates at output nodes of clk0, clk1, clk2 and clk3. These clock pulses of finite durations are use as a clock signals for latches of shift register.

III. PROPOSED METHODOLOGY

Pulse Latch Shift Register: The pulse latch shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals CLK_pulse(1:4) and CLK_pulse(T)). In the 4-bit sub shift register1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register2. Fig. 6 shows the operation waveforms in the proposed shift register.

Four Bit Pulse latch Shift Register: The fig shows the 4 bit pulse latch shift register. It includes 4 latch circuit whose clock signal is connected through pulse clock generator circuit. Clk0, clk1, clk2 and clk3 is connected to the clock input terminal of latch0, latch1, latch2 and clk3 of each latch. The data input which is to be shifted is connected to the input terminal of latch0. The pulse clock generator circuit activates any one of its output clock port. Thus one pulse latch responds to its input terminal at every clock edge of clock pulse generator circuit. Thus data is shifted to its successive latch synchronously.

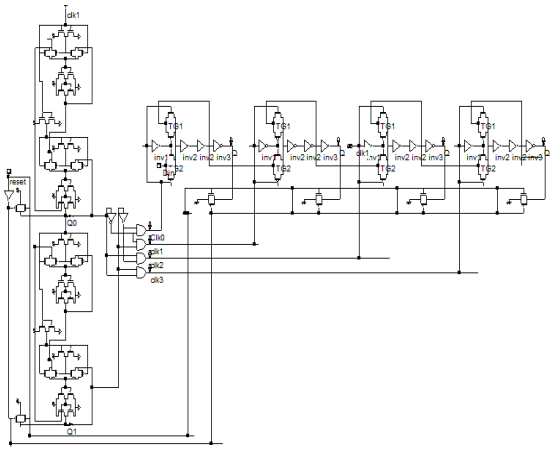

Figure4: Schematic Diagram for 4 bit pulse latch base shift register.

Eight Bit Pulse latch Shift Register: The fig 5 shows the 8 bit pulse latch shift register. It includes 8 latch circuits whose clock signal is connected through pulse clock generator circuit. Clk0 is connected to latch 0 and latch1, clk1 is connected to latch2 and latch3, clk2 is connected to latch4 and latch5 and clk3 is connected to latch 6 and latch 7 respectively.

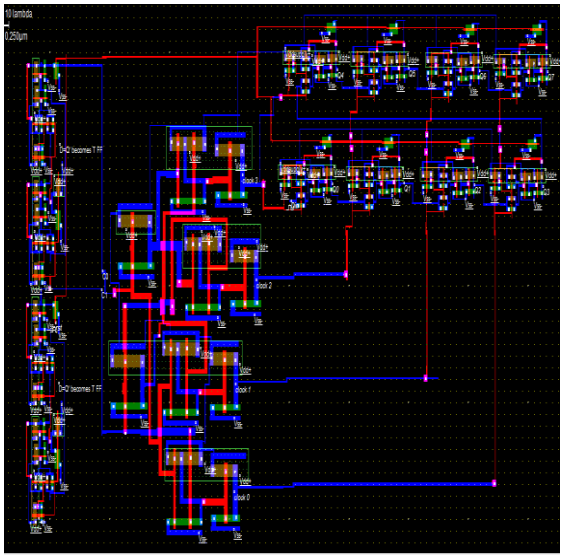

Figure 5: CMOS Layout Design for 4 bit pulse latch shift register

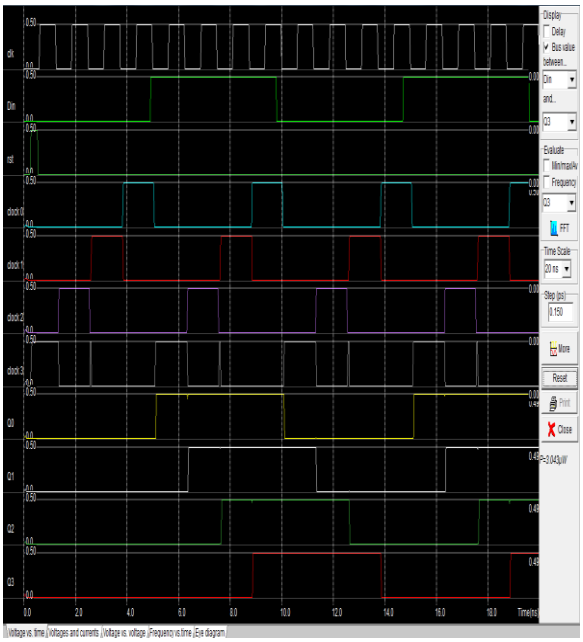

Figure 6: Timing Simulation for 4 bit pulse latch shift register

The timing simulation of 8 bit pulse latch shift register shows the data at input terminal Din is shifted with the arrival of every non overlap clock pulses. The non overlap pulse clock will activates only one latch at a time and the data available at its input terminal is shifted towards the output terminal of that latch.

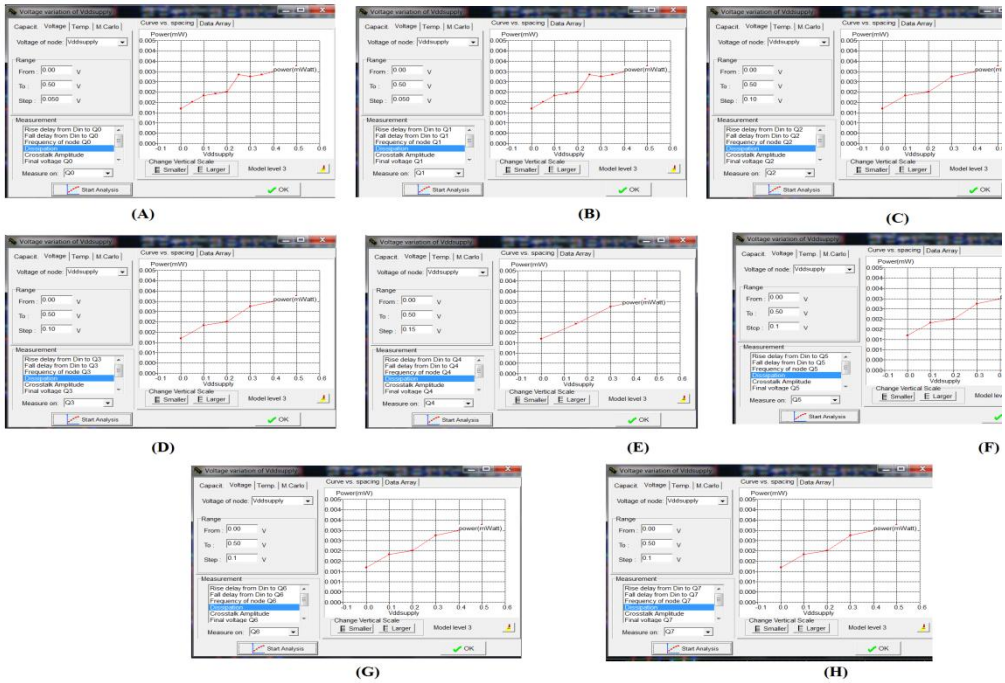

Figure 7: Graphical Analysis of power dissipation at output (A) node Q0 (B) node Q1 (C) Nodes Q2 (D)node Q3 (E) node Q4 (F) node Q5 (G) node Q6 (H) node Q7.

Table I: Comparative Analysis

Type	[1]	This Work
Transistor Size (μm/μm)	NMOS 0.5/1.8 PMOS 0.5/1.8	NMOS 0.05/0.1 PMOS 0.05/0.15
Latch area	19.2 μm^2 (6.7μmX5.6μm)	2.8125μm^2 (2.25μmX1.25μm)
Latch Power Dissipation	3.30 μW	0.209μW
Number of Transistors in Latch	7	10
Word Length	256	256

Total number of Pulse Latch in Shift Register (PLSR)	320	256
Power Dissipation (PLSR)	1.99mW	41.3μW
Area (PLSR)	6600	3162 μm^2 (115 μm X 27.5 μm)

IV. CONCLUSION

This paper discusses the schematic design and its CMOS layout implemetation with optimized area and power of pulse latch base shift register. The simulation analysis shows that the area of latch using 50nm technology is 2.8125 μm^2. The power dissipation for 256 bit length shift register is computed as 41.3μW with the area of 3162 μm^2. The use of transmission gate not only reduces the number of transistors but also optimized the power dissipation of design. The timing problem of pulse latch base shift register is resolve by using the non overlap clock pulses. These pulses are generated from clock pulse generator.

REFERENCES

[1]. Byung-Do Yang "Low-Power and Area-Efficient Shift Register Using Pulsed Latches" IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 62, No. 6, June 2015 pp no 1564.

[2]. Masaki Masuda, Kanto Kubota, Ryosuke Yamamoto, Jun Furuta, Kazutoshi Kobayashi, and Hidetoshi Onodera "A 65 nm Low-Power Adaptive-Coupling Redundant Flip-Flop" IEEE Transactions On Nuclear Science, Vol. 60, No. 4, August 2013 pp no 2750.

[3]. K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera "A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI" IEEE Transactions On Nuclear Science, Vol. 61, No. 4, August 2014 pp no. 1881.

[4]. A.ParvathiKarthica "Power Efficient Synchronous Counter Using Transmission-Gate Based Master-Slave Flip-Flop With Modified Logical Effort Optimization" International Conference on Electronics and Communication Engineering (ECE) 7th April 2013 ppno. 86.

[5]. S. EhsanRazavi, " Shift Register Design Using D-Flip flop with Low Power Consumption and High Speed " International Journal of Science and Advanced Technology (ISSN 2221-8386) Volume 1 No 7 September 2011

[6]. Ch. DayaSagar, T. Krishna Moorthy "Design of a Low Power Flip-Flop Using MTCMOS Technique" International Journal of Computer Applications & Information Technology Vol. 1, No.1, July 2012.