International Journal of Engineering Research and Development
eISSN : 2278-067X, pISSN : 2278-800X, www.ijerd.com
Volume 2, Issue 2 (July 2012), PP. 01-07

Low Power and Improved Read Stability Cache Design in 45nm Technology

K. Dhanumjaya, Dr. MN.Giri Prasad, Dr. K.Padmaraju, Dr. M.Raja Reddy
Jawaharlal Nehru Technological University, Anantapur, AP, INDIA

Abstract*—Cache is fastest memory which is played vital role in the present trend.Cache is achieved by SRAM. The scaling of CMOS technology has significant impact on SRAM cell -- random fluctuation of electrical characteristics and substantial leakage current. In this paper we proposed dynamic column based power supply 8T SRAM cell to improve the read stability and low leakage. In this paper we compare the proposed SRAM cell with respect to conventional SRAM 6T in read mode. To verify read stability and write ability analysis we use N-curve metric. We extract RC parameters of conventional and proposed SRAM cell in read mode. We proved that proposed system is low power in a memory array.Simulation results affirmed that proposed 8T SRAM cell achieved improved read stability, low leakage current and low power in 45nm Technology comparing with conventional 6T SRAM using cadence virtuoso tool.

Keywords*—Cache, SRAM, Leakage Current, N-curve, Read stability, Write-ability, Cadence, Virtuoso, 45nm Technology.

I. INTRODUCTION

For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Technology scaling results in a significant increase in leakage current of CMOS devices. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today.

As process technology is scaled down, threshold voltage variation is increased. In particular, degradation of operating margins in an SRAM memorycellbecomesaseriousproblem.Intheconventional6T cell, it is difficult to find an optimum design because the both read stability and write margin must be considered. At low supply voltage 6T cell worsen in read stability. Leakage power is a high priority consideration due to feature scaling in high performance processor design. In today's processors, the leakage power of cache is a major source of power dissipation because cache occupies more than 50% of the chip area. Low leakage SRAM design leakage SRAM design has been an active area of research over the past years.

In this paper, we use dynamic cell supply 8T SRAM cell to address the above problems. We compare the conventional 6T and proposed 8T SRAM cell with respect to read stability and leakage.

The rest of the paper is organized as follows:

Section II presents stability analysis using N-curve. Section III reviews the basic operation of conventional 6T SRAM cell. Section IV presents the proposed cache design [1] and its circuit implementation. Section VpresentsCadence design flow. Section VI presents simulation results. Section VII represent conclusion of the paper.

II. STABILITY ANALYSIS USING N-CURVE

A. Read Stability

The cell becomes less stable with lower supply voltage, increasing leakage currents and increasing variability, all resulting from technology scaling. The stability is usually defined by the SNM as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without change the stored bit. Locating the smallest square between the two largest ones delimited by the eyes of the butterfly curve determines graphically the SNM shown in Fig1.

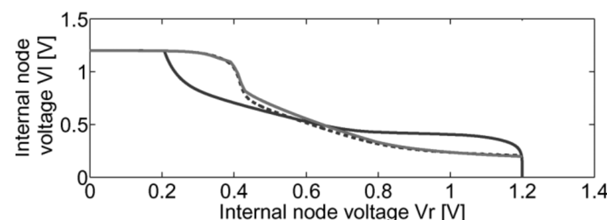
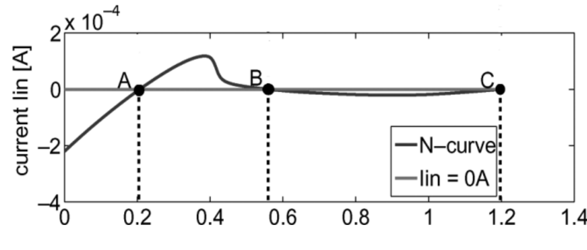


Fig 1: SNM

The drawback of the SNM is the inability to measure the SNM with automatic inline testers, due to the fact that after measuring the butterfly curves of the cell the static current noise margin (SINM) still has to be derived by mathematical manipulation of the measured data. An alternative definition for the SRAM read stability is based on the N-curve of the cell, which is measurable by inline testers. The combined voltage and current information provided by the N-curve (Fig.2) [2].

The voltage difference between point A and B indicates the maximum tolerable DC noise voltage of the cell before its content changes. This voltage metric is the static voltage noise margin (SVNM). The additional current information provided by the N-curve, namely the peak current located between point A and B, can also be used to characterize the cell readstability. This current metric is the static current noise margin (SINM).



Voltage in internal node in (V)

Figure 2. N-curve of the cell.

B. Write Stability

Besides the read stability for the SRAM cell, a reasonable write-trip point is equally important to guarantee the write-ability of the cell without spending too much energy in pulling down the bit-line voltage to 0 V. The SRAM N-curve can also be used as alternativefor the write-ability of the cell, since it gives indications on how difficult or easy it is to write the cell. The negative current peak(Fig 2) between point C and B or the write-trip current (WTI) is the amount of current needed to write the cell when both bit-lines are kept at VDD. Similarly, the voltage difference between point C and B or the write-trip voltage (WTV) is the voltage drop needed to flip the internal node "1" of the cell with both the bit-lines clamped to VDD.

The N-curve current information is critical for designing a cell in nanometer technologies. Moreover, it allows overcoming the read stability limit of 0.5VDD. Finally, to find the stability of the system we should consider the SVNM, SINM, WTV and WTI.

III. CONVENTIONAL 6T SRAM CELL

A. Construction

Fig 3 shows the conventional 6T SRAM cell which has two back to back connection of inverters using N1, P1, N2, P2 to store the single bit either '0' or '1'. N3, N4 transistors are called as access transistors. WL is used to turn ON the access transistors. BL, /BL are bit lines.

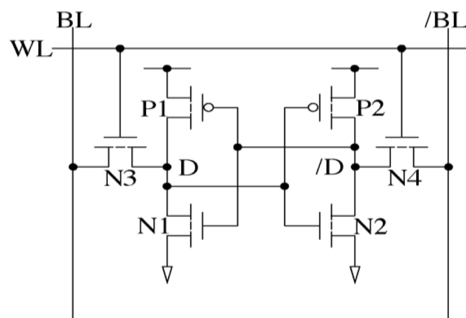


Fig 3. conventional 6T SRAM cell.

B. Operation

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

- **Standby:** If the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two cross coupled inverters formed by P1-N1, P2-N2 will continue to reinforce each other as long as they are connected to the supply.
- **Reading:** Assume that the content of the memory is a 1, stored at D. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.
- **Writing:** The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of

the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters.

IV. PROPOSED DYNAMIC 8T SRAM CELL

A.Construction

The proposed SRAM cell consists of 8 transistors, N1-N5 and P1-P3, as shown Fig.4. Four transistors N1, N2, P1, P2form a cross-couple structure to store data. Four transistors P3 and N3-N5 are access to the internal nodes D and /D. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply(*cell_supply*) line which is raised to the higher voltage during read operation to obtain a higher noise margin.

B. Operation

Like conventional 6T SRAM, it has three modes of operations*: standby, read and write* as follows

- **Standby:** During standby, *Cell_Supply* voltage is kept at VDD to maintain a high noise margin.at the same time WL is pre-charged high while all CS is pre-charged low. As a result, transistor N5 of cell is tured on to pre-charge node C1 to ground. Thus, both access transistors N3 and N4 turned off,isolating the storing element from any BL disturbances. Also, BLs are pre-charged to VDD to prepare for the next read/write operation.
- **Reading:**read operation starts by raising CS from ground to VDD and *Cell_Supply*is raised from VDD to VDD2. VDD2 must be higher than VDD to improve noise margin of cell during read operation. At the same time WL is pulled to low to drive node C1 to VDD and hence turning on N3 and N4. Once N3 and N4 are turned on to read the cell data, subsequent circuit operation same as the conventional 6T SRAM.
- **Writing:** Write operation of the proposed design is much simpler than its read operation. Write operation starts by asserting CS line to VDD while the WL is pulled down. Meanwhile, one of the BLs is pulled to ground while other kept at VDD. When node C1 is charged up to VDD, both N1 and N2 are turned on and input data is written into memory similar to conventional 6T SRAM.

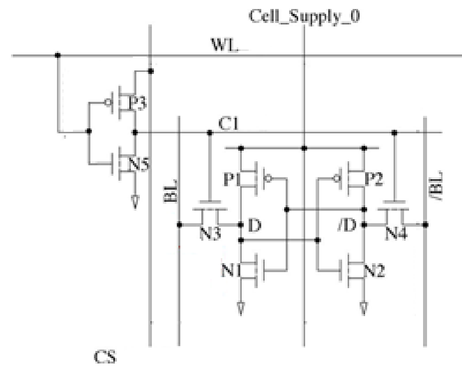


Fig 4. proposed 8T SRAM cell.

V. PROPOSED SYSTEM ARRAY DESIGN

Designing of an array is necessary to prove that proposed system is consuming less power comparing with conventional array design.Fig 5 shows the array architecture of proposed system .

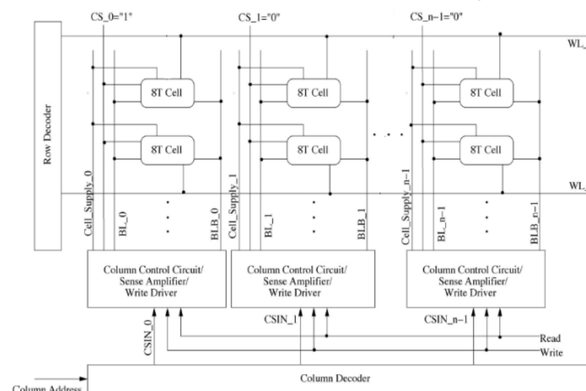


Fig 5. proposed system array design.

By using a dynamic cell supply scheme coupled with a special access topology, the proposed design requires extra wiring as well as power consumption in the column control circuit.it consumes more power than the conventional 6T design at the same operating voltage and frequency. TheCell_Supply signal driven from VDD to VDD2 in read operation. The additional power dissipation is proportional to the parasitic capacitance of the Cell_Supply line and the voltage swing. However, since only one cell on a row is activated during each read/write cycle, power saving from this special feature can be used to compensate the above-mention drawbacks. Proposed system has peculiar property which is isolating the eachbit cell using CS and WL signals.In this paper we design 1kb SRAM array to check power consumption.

VI. CADENCE DESIGN FLOW

Cadence design Systems is electronic design automation software and engineering Services Company that offers various types of design and verification tasks that include:

- **Virtuoso Platform** - Tools for designing full-custom integrated circuits, includes schematic entry, behaviouralmodelling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation. Used mainly for analog, mixed-signal, RF, and standard-cell designs.
- **Encounter Platform -** Tools for creation of digital integrated circuits. This includes floor planning, synthesis, test, and place and route. Typically a digital design starts from Verilog netlists.

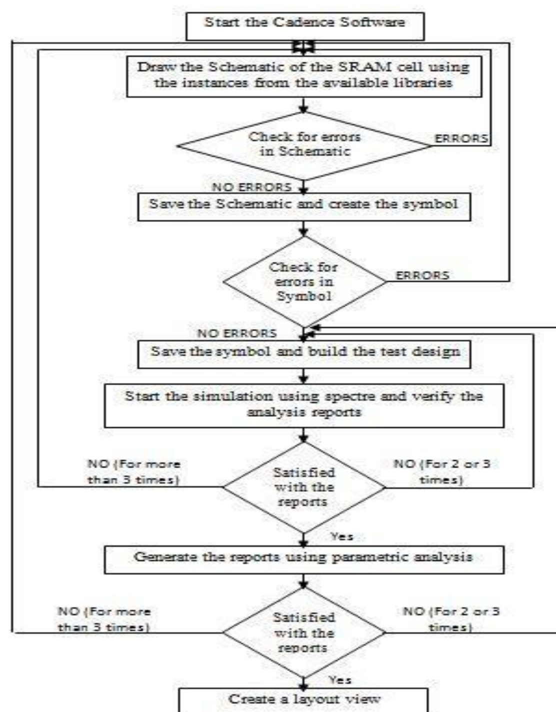


Fig 6. cadence virtuoso design flow.

- **Incisive Platform -** Tools for simulation and functional verification of RTL including Verilog, VHDL and System C based models. Includes formal verification, formal equivalence checking, hardware acceleration, and emulation.

The proposed work is done in Virtuoso platform using gpdk45 nm technology. The flow of design is as shown in figure 6. Using above flow we design necessary circuits such as both conventional and proposed bit cells, 5 to 32 decoder, sense amplifier circuits in cadence virtuoso schematic tool. Fig 7 & Fig 8 shows the bit cell schematic for conventional 6T and proposed 8T using cadence virtuoso schematic editor. After that we create symbols for both and analysis those cells in various aspects.

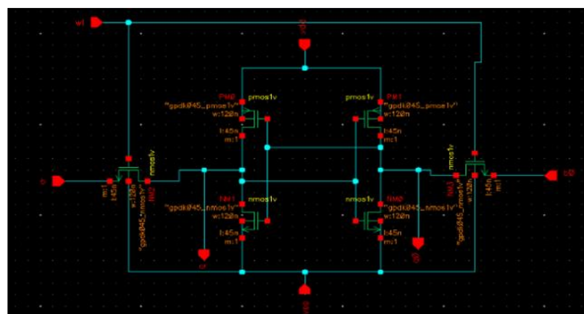


Fig 7. Conventional 6T SRAM cell design in cadence

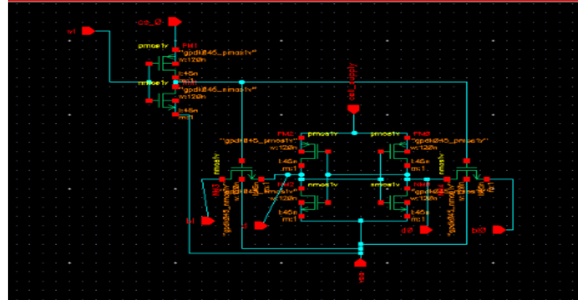


Fig 8.proposed 8T SRAM cell design in cadence.

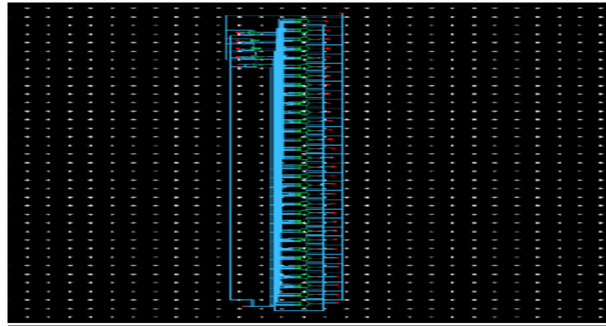


Fig 9. 5 to 32 decoder design in cadence.

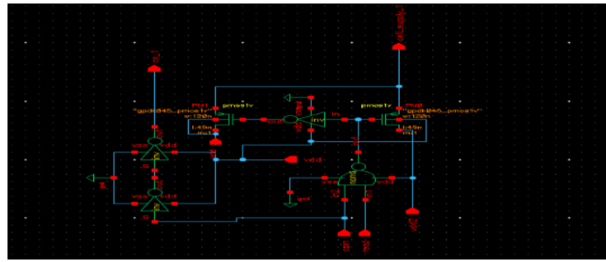


Fig 10.Sense amplifier design in cadence.

Fig.9 shows the decoder design in cadence since we are designing 1kb cache we need to organize bit cells as 32*32 array design for column as well as row we use the 32 decoder.

Fig.10 shows the sense amplifier design in cadence which can used to sense the bit lines.

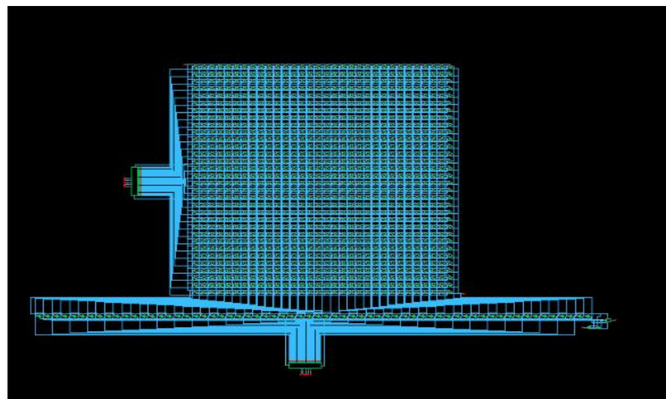


Fig 11. Conventional 6T SRAM array design in cadence

Fig.11 & Fig.12 shows the conventional 6T and proposedSRAM array design after creating the schematic create a symbol to test the array.

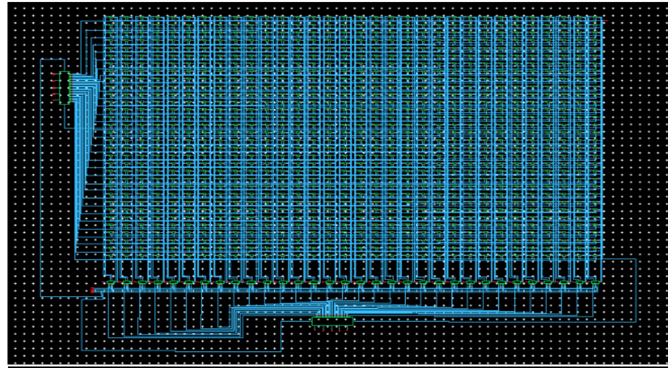


Fig 12. Proposed 8T SRAM array design in cadence

VII. SIMULATION RESULTS

Cadence spectra simulation of DC analysis gave good results. The results are shown in below Table I. We compare SRAM cells using DC simulations shown from Fig 8 to Fig 11.

Table I Summary of Conventional 6T and Dynamic 8T bit cells results

	Conventional SRAM 6T	**Proposed SRAM 8T**
CMOS Process	45nm/1V	45nm/1V
Read/write process	Differential	Differential
SVNM	325mV	668.6mV
SINM	35.61 µA	98.16 µA
WTV	475mV	487.8mV
WTI	-10.47µA	-48.35µA
Leakage current	10.026fA	5.21143fA
Read current	5.39421pA	99.5612µA

A. SRAM 6T cell analysis results

We analysis the read stability of SRAM cell with respect to N-curve as shown in fig 13. It gives us the SVNM,SINM,WTV,WTI.

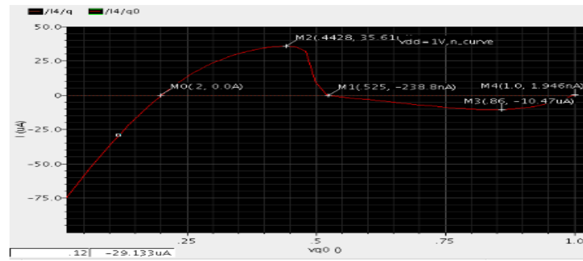


Fig 13. 6T SRAM cell N-curve.

Below fig .14 shows the leakage current calculation process in read operation.

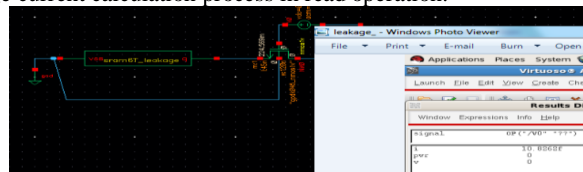


Fig 14. leakage current of 6T SRAM cell in read operation.

B. Proposed SRAM 8T cell analysis results.

Fig.15 shows the N-curve of 8T SRAM cell, by observing the curve we come to decide that read stability was improved over the conventional 6T SRAM.

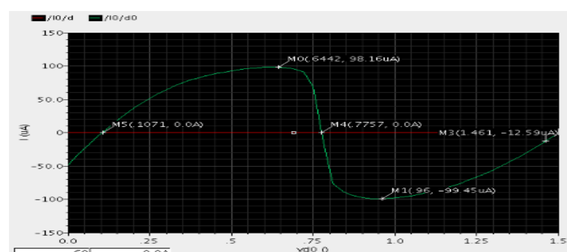


Fig15. N-curve of proposed 8T SRAM cell.

Leakage current finding procedure as shown in below Fig .16, compare to conventional 6T the proposed 8T SRAM cell has less leakage current.

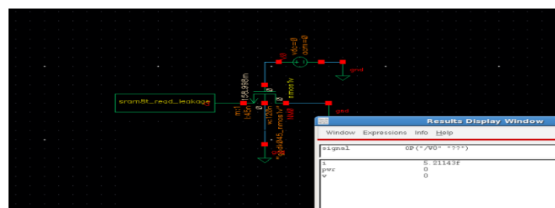


Fig16. Leakage current of 8T SRAM in read operation.

Below fig 17 gives information about the power consumption of 1kb cache array. We achieve almost 54% power reduction.

Table III Summary of Conventional 6T and Dynamic 8T 1kb array power consumption results

	Conventional SRAM 6T	**Proposed SRAM 8T**
Power consumption	1.12094mW	519.1476µW

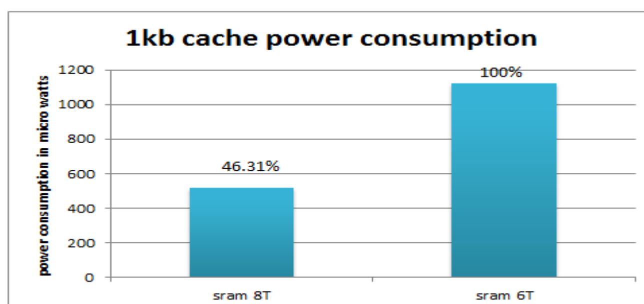


Fig 17. 1kb cache power consumption comparasion.

VIII. CONCLUSION

A 8T SRAM with a column-based dynamic supply has been proposed. Analyse both conventional 6T and proposed SRAM using N-curve. The proposed SRAM 8T cell has achieved improved read stability, low power, read current and leakage current. N-curve metric was best method to analysis the cell stability it contains both voltage and current information. So, we can analysis the cell stability correct way. Above results prove that 54% of the power is reduced and read stability of proposed cell achieve double amount approximately with comparing SRAM 6T cell.

REFERENCES

[1]. Do Anh-Tuan, Jeremy Yung Shern Low, Joshua Yung Lih Low, Zhi-Hui Kong, Xiaoliang Tan, and Kiat-SengYeo,"An 8T Differential SRAM With Improved NoiseMargin for Bit-Interleaving in 65 nm CMOS" IEEE Transnctions on circuits and systems—I :regular papers, Vol. 58, No. 6, june 2011.

[2]. E. Grossar*et al.*, "Read stability and write-ability analysis of SRAM cells for nanometer technologies," *IEEE J. Solid-State Circuits*, vol.41, no. 11, pp. 2577–2588, Nov. 2006.

[3]. A. Sil*et al.*, "A novel 8T SRAM cell with improved read-snm," in *Proc. NEWCAS*, 2007, pp. 1289–1292.

[4]. Jan M. Rabaey,AnanthaChandrakasan and BorivojeNikolic, "Digital Integrated Circuits", ISBN 81-7808-991-2, Pearson Education, 2003.

[5]. Neil H.E.Weste,David Harris and Ayan Banerjee, "CMOS VLSI Design, a circuits and systems perspective" ,ISBN: 0321149017/9780321149015Third edition, Pearson Education, 2005.