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Design and Simulation of BPSK Demodulation at Low Bit Rate

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Abstract:- This paper presents BPSK Demodulation at Low Bit Rate. BPSK demodulation designed such that has 4 inputs: Bit rate, Carrier frequency, Sampling frequency and Input modulated Bit stream are user controllable. In future this design will help to compare results of BPSK Demodulation that was going to implement on STRATIX III FPGA Dsp Development Board.

Keywords:- BPSK, FPGA, Low Bit Rate, BPSK Demodulation, Bits per second.

I. INTRODUCTION

Now days, a major transition from analog to digital modulation techniques has occurred and it can be seen in all areas of satellite communications systems. A digital communication system is more reliable than an analog. The aim of the paper is to create a BPSK (Binary Phase Shift Keying) Demodulator which demodulates the Modulated signal comes from Modulator which has Bit rate 1200 bps. First we give Introduction about BPSK Demodulation and then BPSK Demodulation is designed and Implemented in Matlab. In this Design of BPSK Demodulation Bit Rate, Carrier frequency, sampling frequency are User controllable. This paper presents extended work of RTL Design and Implementation of BPSK Modulation at Low Bit Rate .In this BPSK Modulation is Design and Implement at low Bit Rate 1200 bps[1].

II. THEORETICAL BACKGROUNDS

DIGITAL COMMUNICATION SYSTEM

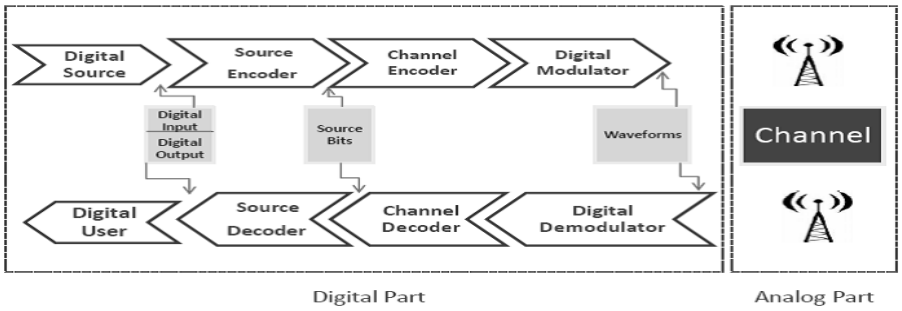

Fig.1: Digital Communication System [2]

Block Diagram of Digital Communication System is shown in Fig.1.Digital communication system is mainly divided in two parts digital and analog. The digital part of this communication system consists of digital source/user, source encoder/ decoder, channel encoder/ decoder and the digital modulator/ demodulator. The analog part is consist of the transmitter, receiver, the channel models and noise models [3].The message to be sent is from a digital source then source encoder accepts the digital data and prepares the source messages. The role of the channel encoder is to map the input symbol sequence into an output symbol sequence. The binary information obtained at the output of the channel encoder is than passed to a digital modulator which serves as interface with the communication channel. The main purpose of the modulator is to translate the discrete symbols into an analog waveform that can be transmitted over the channel [4], [5]. In the receiver, the reverse signal processing happens. A channel is the physical medium that carries a signal between the transmitter and the receiver. The signal is corrupted with noise whatever the medium used for transmission The digital data is transmitted between the transmitter and the receiver by varying a physical characteristic of a sinusoidal carrier, either the frequency or the phase or the amplitude in our case sinusoidal carrier is vary according to phase. This

operation is performed with a modulator at the transmitting end to impose the physical change to the carrier and a demodulator at the receiving end to detect the resultant modulation on reception [6].

A. Concept of BPSK Demodulation

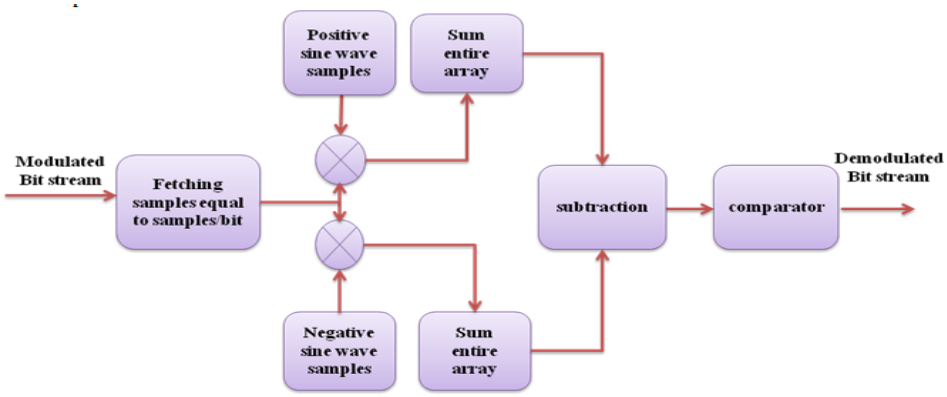

Fig.2: Principal of BPSK Demodulation

In BPSK demodulator design modulated bit pattern is given as Input. Samples per bits are fetched in sequence. Then samples of one bit is fetched from Modulated Pattern, are multiplied with Positive and Negative carrier samples. Sum of multiplication output will store in two different arrays. Subtraction block will perform subtraction of two different array in which sum of multiplication output is stored. Comparison block do the comparison based on output of subtraction block. If subtraction of samples is grater then zero then bit"1" is detected and if subtraction of samples is less then zero then bit "0" is detected at output of demodulator.

III. DESIGNING OF BPSK DEMODULATION

The Matlab BPSK demodulation designed has 4 inputs: Bit rate, Carrier frequency, Sampling frequency and Input modulated Bit stream (to be demodulated). BPSK Demodulation is designed such that all the input parameters can have variable values, thus making it a generic BPSK demodulator.

As shown in the block diagram, samples per sine wave are determined by dividing sampling frequency with the carrier frequency. No of sine waves per bit is determined by dividing Carrier frequency with the bit rate. No of samples per bit is determined by dividing Sampling frequency with the bit rate. Once we have the samples per sine wave required, we divide the 0 to 360 degrees in that no of values for representing 1 sine wave. Then we take sine of all above values and store it in an array making 1 sine wave to represent modulated bit 1 while take –sine of all above values and store it in another array making 1 sine wave (180 degree phase shift) to represent modulated bit 0.

Then we create two arrays in which in we append sine waves per bit times the array representing 1sine wave (0 degree and 180 degree phase shifted) to get 1 bit modulated sine wave signal for bit 1 and for bit 0.From input modulated bit stream we fetch values equal to number of sample per bit and store it in an array.

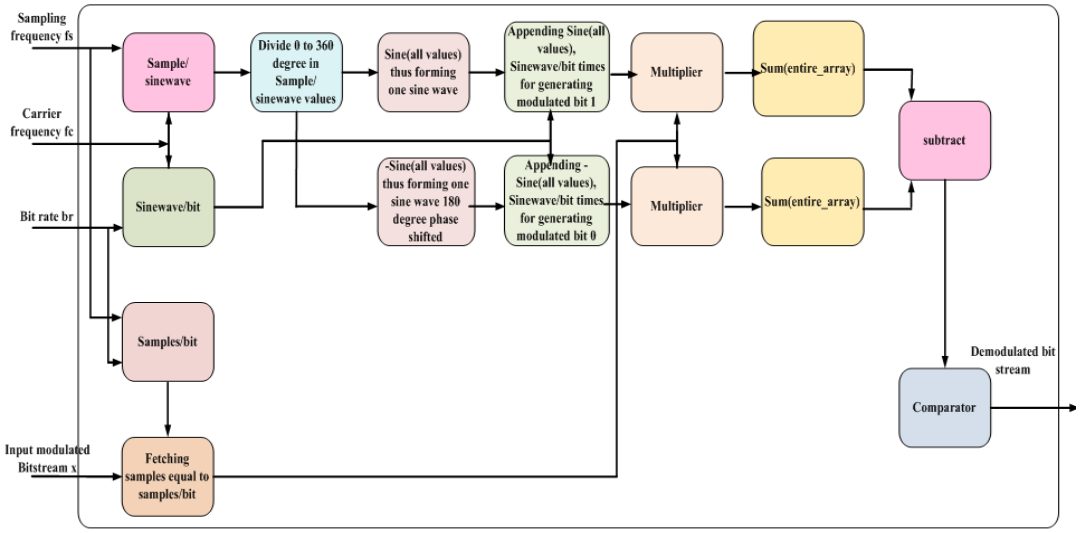

Fig.3: Design of BPSK Demodulation

Then we multiply the above array containing samples of BPSK modulated bit with the two arrays representing modulated bit 1 and bit 0.Each element of the multiplied output of both array are summed in two respective variables. They are then subtracted, if value is greater than zero than bit is detected 1 else 0.The value will be equal to either positive or negative of no of samples per bit. If it is positive then bit detected is 1 else 0.

IV. SIMULATION RESULTS

The simulated results are obtained for three different Bit rates, Carrier frequency, sampling frequency and Input modulated Bit stream.

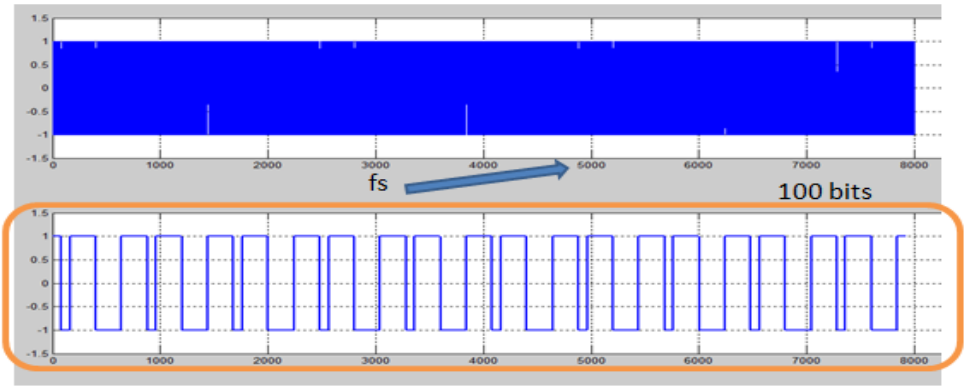

Fig.4.1: Simulation for BPSK Demodulation when Bit rate=100, fc=1000Hz, fs=8000Hz

Fig 4.1 shows output when Bit rate is 100, carrier frequency is 1000Hz and sampling frequency is 8000Hz.In this fig we can see that there are 100 Demodulated Bits at output of BPSK Demodulation when Bit rate is 100 and Input modulated Bit Pattern 1100110 is repeat which is received at output.

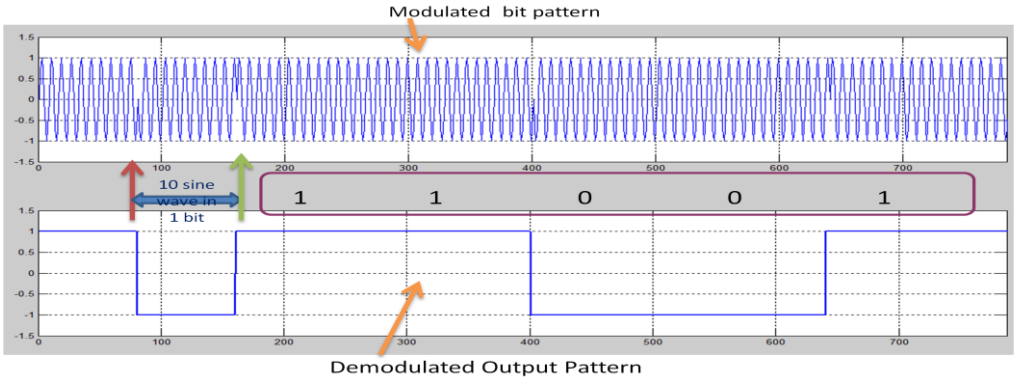

Fig.4.2: Simulation for BPSK Demodulation when Bit rate=100, fc=1000Hz, fs=8000Hz

Fig.4.2 shows zoom in view of Fig 4.1.From Fig 4.2 we can obtain carrier frequency when multiplication of number of sine waves per bit and Bit rate is taken, Here Bit rate is 100 and 10 sine waves per bit and so carrier frequency becomes 1000Hz.

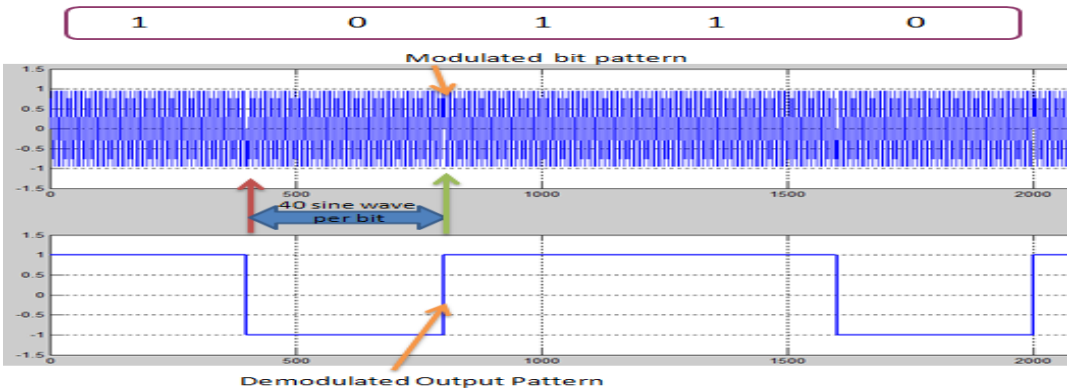

Fig.5 : Simulation for BPSK Demodulation when Bit rate=1200, fc=48 KHz, fs=480 KHz

Fig 5.shows output when Bit rate is 1200, carrier frequency is 48KHz and sampling frequency is 480KHz and Input modulated Bit Pattern is 10110.Here Bit rate is 1200 and 40 sine waves per bit and so carrier frequency becomes 48KHz.

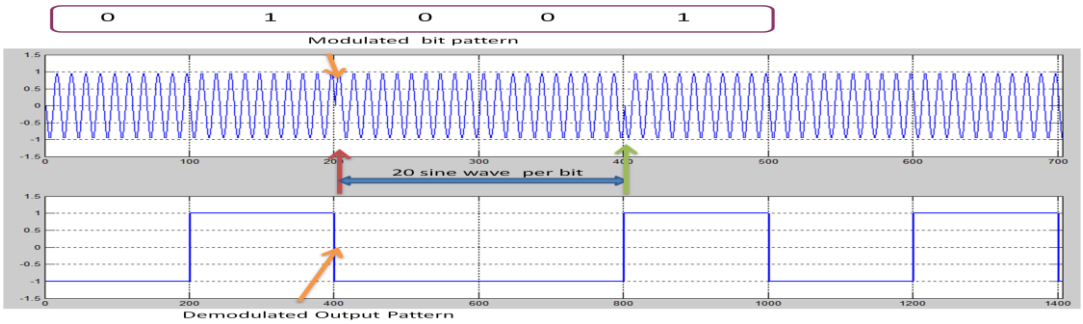

Fig.6 : Simulation for BPSK Demodulation when Bit rate=600, fc=12 KHz, fs=120 KHz

Fig 6.shows output when Bit rate is 600, carrier frequency is 12KHz and sampling frequency is 120KHz and Input modulated Bit Pattern is 01001.Here Bit rate is 600 and 20 sine waves per bit and so carrier frequency becomes 12KHz.

V. CONCLUSIONS

In this paper, simulated results are presented for the three different bit rate, carrier frequency, and sampling frequency. From these results we can see that carrier frequency, sampling frequency and bit rate are user controllable. This results are finally used to compare output results of BPSK demodulation at low bit rate which is going to Implement on StratixIII FPGA.

REFERENCES

[1] Nehal.A.Ranabhatt, Sudhir Agarwal, Priyesh.P.Gandhi, "RTL Design and Implementation of BPSK Modulation at Low Bit Rate", International Journal of Engineering Research & Technology, Vol.2, Issue 28, Feb 2012.

[2] S.O. Popescu, A.S.Gontean and G.Budura "BPSK System on Spartan 3E FPGA" SAMI 2012 • 10th IEEE Jubilee International Symposium on Applied Machine Intelligence and Informatics • January 26-28, 2012.

[3] A.Gürgör, F.Arikan, O.Arikan, "Simulation of a digital communication system", in Proceedings of the 13th European Signal Processing Conference EUSIPCO, 2005, Turkey,http://www.eurasip.org/Proceedings/Eusipco/Eusipco2005/defevent/papers/cr1142.pdf

[4] H.Nguyen, E.Shwedyk, A first Course in Digital Communications, Cambridge University Press, New York, 2009.

[5] J.G. Proakis, Digital Communications, 4th edition, McGraw Hill, New York, 2001.

[6] G. Smithson, "Introduction to Digital Modulation Schemes", in IEE Colloquium on The Design of Digital Cellular Handsets, 1998, United Kingdom, pp. 2/1 - 2/9