International Journal of Engineering Research and Development
e-ISSN: 2278-067X, **p**-ISSN: 2278-800X, www.ijerd.com
Volume 7, Issue 12 (July 2013), PP. 01-09

Design and Implementation of New Full-Bridge Single-Stage Converter Topology

K.Kartheek Kumar Naidu[1], G.KrishnaDeekshit[2]
[1]PG Student (PE&ED) Department of Electrical & Electronics Engineering S.V.P.C.E.T., Puttur
[2]ASSISTANT PROFESSOR Department of Electrical & Electronics Engineering S.V.P.C.E.T., Puttur

Abstract:- This paper presents a single-stage circuit topology consisting of the association of a full-bridge isolated dc–dc converter and two input inductors and two input diodes connected to the mains network, in order to obtain an isolated ac/dc switch mode power supply, with sinusoidal input current. The proposed topology does not use an input bridge rectifier, common in similar applications. The current in the two input inductors can therefore, flow in both directions. Consequently, the proposed topology equally distributes the current by the four-bridge transistors that provide four input parallel boost power factor correctors (PFCs). The use of the four-bridge permitting the accurate simultaneous regulation of output voltage and input current is hereby described. The inter-dependency between these two conversion processes is completely analysed, allowing for useful design rules. Simulation results of conventional and proposed single stage converter topology are obtained. A maximum efficiency of 94% was obtained transistors to obtain the PFC function and regulate the output voltage with galvanic isolation is a new technique that makes this topology unique, which also contributes to improve the converter efficiency.

Index Terms:- Full-bridge converters, input current shaping, low-distortion input current, single-stage power factor correctors (PFCs).

I. INTRODUCTION

In modern switch mode power supplies (SMPSs) with galvanic isolation, the capacity to perform power factor correction (PFC) is a frequent characteristic, in compliance with the standard IEC-1000-3-2. This requirement is normally achieved with an additional input converter, typically a bridge rectifier, followed by a boost converter [1]–[3]. For high power levels, the association of this input converter with the full-bridge isolated dc–dc converter results in a two stages converter with the inherent characteristics: high cost and the necessity of having very high efficiency in each stage. It should be noted that, to obtain a global efficiency greater than 95% is necessary that each stage presents efficiency greater than 97.5%, which may be difficult and also expensive to obtain, when the second stage is a full-bridge converter.

Recently, new PFC bridgeless promising solutions, mainly intent to replace the input rectifier and the boost converter, have emerged [4]–[7]. These techniques were permitted to obtain good input current wave shaping with lower harmonic distortion and efficiency higher, >95%, than the ones presented in [1]–[3]. However, to perform also high-frequency isolation and output dc voltage regulation, these topologies still need the presence of another converter (an isolated dc–dc converter). Thus, the overall system will result in a high-cost two-stages converter, gaining only an increase in the efficiency, when compared with the topologies presented in [1]–[3]. Consequently, these topologies are not suited for the application focused in this paper, which is based in one-stage converter.

Considering the constant interest of the industry in reducing the cost and the increase of efficiency of the SMPS, while maintaining the PFC function, several topologies of isolated ac/dc single-stage SMPS have been proposed, based on the forward and flyback dc–dc converters for low-power applications [8]–[17]. However, in the case of high-power applications, the voltage and current ratings of the power transistor and diodes increase considerably, thereby rising the cost of these solutions to values that can be even higher than those observed in the two-stages topologies [18]. In view of the power limitation of these topologies, single-stage isolated full-bridge topologies with PFC function have been proposed recently [19]–[28].

These topologies can perform input current wave shaping and output voltage control, simultaneously, without using any additional transistors. However, these topologies are not optimized in terms of additional components and current distribution in the bridge transistors. For example, in the topologies presented in [19]–[28], only two parallel input boost converters are provided using the low-side transistors, which leads to asymmetrical current distribution in the bridge transistors causing, in these transistors, a high current stress. An input bridge rectifier is also needed for these topologies. For the topologies proposed in [19]–[24], only one input inductor is used, but this inductor and the two low-side transistors have to support the maximum input current. On the other hand, the topology presented in [25]–[28] uses two inductors for half of the maximum input current, which means that, each low-side boost transistor needs only to support half of the maximum input

current, thereby reducing the current stress in these transistors. However, the topology uses six additional diodes, thus increasing the cost and reducing the efficiency.

In an attempt to solve the referred problems, this paper presents an optimized and improved single-stage full-bridge ac/dc converter, where the input bridge rectifier was replaced by two rectifier diodes (see Fig. 1).

This fact obviously allows, by itself, a slight improvement in the converter efficiency. In addition, it also guarantees the improvement of the converter by performing four input boosts, to accomplish the PFC function (see Fig. 2), instead of two as it is common in other existing topologies. This way, the operation of the proposed topology will result symmetric, with all the inherent advantages in terms of current and voltage switches' stress reduction.

Full analysis and design criteria are completely described in the paper. Finally, a 650-W prototype, with an input voltage range of 180–250 V_{rms} and an output voltage of 48 V dc, was designed and built to verify the theoretical analysis and evidence the converter performance. The developed prototype achieves a maximum efficiency of 94% at full load.

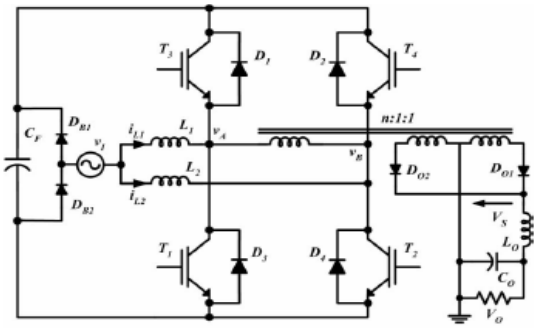

Fig.1. High-efficiency full-bridge single-stage topology.

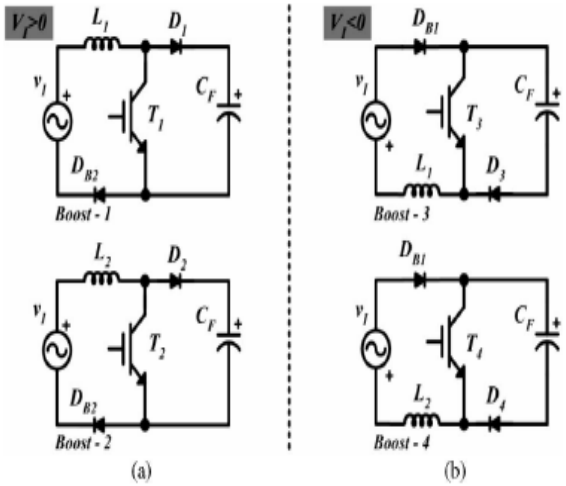

Fig.2. Four boost converters provided by the topology. (a) low-side transistors and (b) high-side transistors.

In summary, the main original contribution of this paper consists of the introduction of a full-bridge single-stage SMPS evidencing reduced number of additional components to provide four input boost converters with symmetrical current distribution through all the bridge transistors. This contributes to decrease the cost and increase the efficiency, thus turning this topology attractive to the industry. The paper also includes the full description, analysis, and design of the proposed topology.

II. OPERATING PRINCIPLES AND TOPOLOGY ANALYSIS

This section introduces the most important theoretical concepts that govern the operation of the output voltage v_s transistors gate signals for different input duty ratios and currents in L1and L2 for $v_I > 0$.
proposed converter, namely, the input current wave shaping and the output voltage regulation. The study is based on the definition of the two inherent duty ratios, D_O and D_I, necessary to obtain the simultaneous control of the output voltage and the input current. The performed analysis has also the objective of defining the minimum value of the V_{CF} voltage that permits the correct converter operation.

The new input configuration used provides four input boost converters: two performed by the low-side transistors (T1 and T2) when $v_I > 0$, and other two by the high-side transistors (T3and T4) when $v_I < 0$, see Fig.2. As aforementioned, the capacity of accomplishing two different conversion

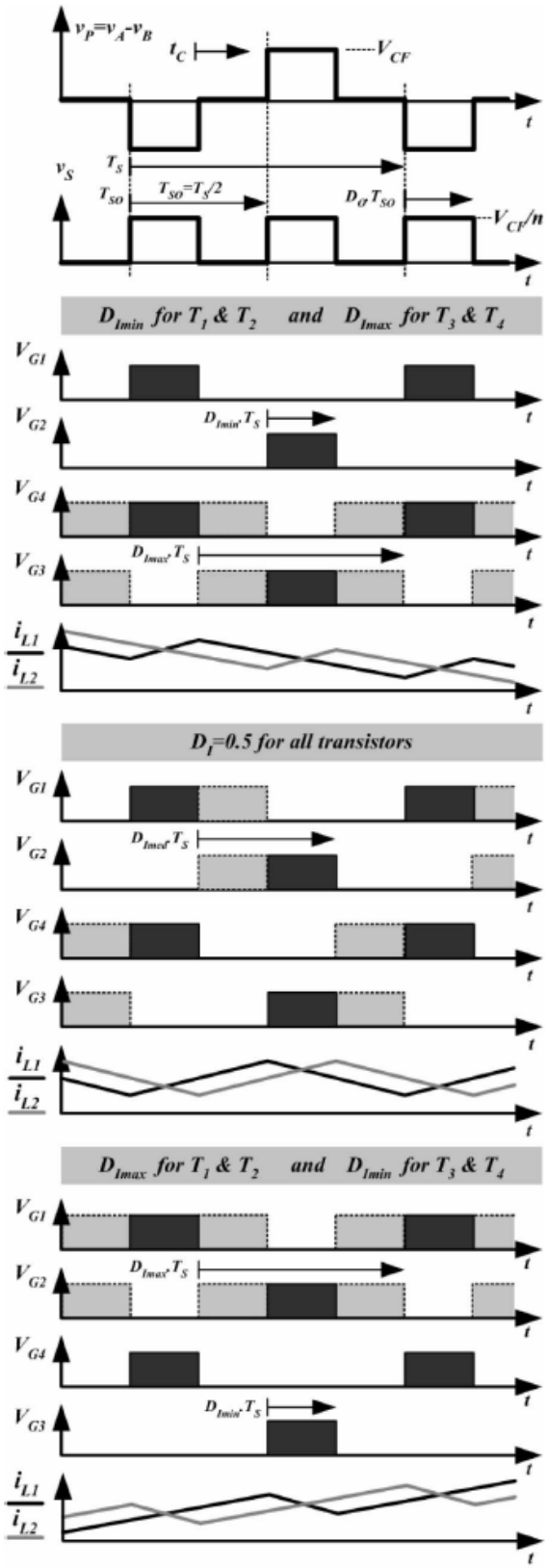

Fig.3. Transformer primary voltage v_p rectified

TABLE I
POWER TRANSISTORS' SWITCHING STATES

T_1 / T_3	T_2 / T_4	$v_P = v_A - v_B$	state/time	i_{L1}	i_{L2}
on/off	on/off	0	S_{00}/t_{00}	↑	↑
on/off	off/on	$-V_{CF}$	S_{01}/t_{01}	↑	↓
off/on	off/on	0	S_{11}/t_{11}	↓	↓
off/on	on/off	$+V_{CF}$	S_{10}/t_{10}	↓	↑

processes in only one stage results from the possibility of having two different duty ratios: D_I, to control the input current (input duty ratio, in a period time T_S, referred to the primary transformer voltage v_P) and D_O, to control the output voltage (output duty ratio, in a period time $T_{SO} = T_S /2$, referred to the output rectified voltage v_S), see Fig. 3. The output duty ratio DO controls the conduction of two transistors of the same diagonal, i.e., the conduction of T_1 and T_4 or T_2 and T_3. The input duty ratio D_I controls the conduction of the two low-side transistors T_1 and T_2 when $v_I > 0$ or the two high-side transistors T_3 and T_4 when $v_I < 0$.

As it is usual in full-bridge single-phase inverters, this topology also allows four switching states. Table I summarizes the switching states of the power transistors and their respective conduction times, where v_A and v_B are the collector voltages of transistors T_1 and T_2 , respectively, and v_P the voltage at the transformer primary terminals ($v_P = v_A – v_B$). The influence of the converter states into both inductors' currents is also presented in Table I.

Before starting the explanation of the full-bridge and boosts power conversion processes, it is necessary to introduce some important concepts related to the two respective duty ratios and their range of variation. In the following analysis, it is considered that the output filter operates in continuous conduction mode (CCM).

The input duty ratio DI is obtained by the input current controller, which selects the appropriate states S_{00} or S_{11}, during the time interval where $v_P = 0$, i.e., when there is no energy transfer to the output filter. This time interval, marked as t_C in Fig. 3, is then used to provide the input current shaping.

The adoption of the states S_{00} or S_{11} results in a discrete variation of the input-duty ratio, leading to three possible values, D_I min , D_I med , and D_I max [see (1)–(3)]. Fig. 3 shows the three input duty ratios considering the same output duty ratio D_O. Additionally, the selection of the states S_{00} or S_{11} during the interval time t_C has no influence in the rectifier output voltage and the transformer primary voltage. The evolutions of the input inductors currents, i_{L1} and i_{L2}, for the three possible input duty ratios are also presented in Fig. 3 (considering $v_I > 0$). The output duty ratio DO is imposed by the output voltage regulation. Therefore, it cannot be changed in order to control the input current shape. This fact introduces a restraint in the input duty ratio D_I, i.e., considering a range of variation for D_O, a range of variation is obtained for DI that depends directly from D_O. On inspecting Fig. 3, it is possible to establish the relations between the input duty ratio D_I and the output duty ratio D_O.

$$D_{I\min} = \frac{D_O}{2} \qquad (1)$$

$$D_{I\mathrm{med}} = 0.5 \qquad (2)$$

$$D_{I\max} = 1 - \frac{D_O}{2}. \qquad (3)$$

As stated before, the control strategy for the input current consists of the selection between the states S_{00} and S_{11} during time interval t_C. Adopting the state S_{00} (T_1 and T_2 ON), the input inductors' currents increase, while adopting S_{11}, both currents decrease (T_3 and T_4 ON).

It is possible to obtain a linear and continuous variation of the input duty ratio, which means that the states S_{00} and S_{11} can be changed during the time interval t_C , but this mode of operation increases the switching losses and does not results to a considerable improvement of the input current wave shaping. This way a discrete operation was adopted instead.

To enable the operation of the converter, the dc voltage across the capacitor C_F must satisfy some conditions. Considering a sinusoidal input voltage that supplies the boost converters performed by the circuit presented in Fig. 1, and having in mind the conversion ratio of the conventional dc–dc boost converter, the voltage at the capacitor C_F terminals must verify condition (4) to guarantee the boost operation during all the mains voltage period:

$$V_{CF} \geq VImax \sin(\omega t) \frac{1}{1-DI} \qquad (4)$$

Considering the worst situation that occurs at $\omega t = \pi/2$, and the relation between $D_I = D_I$ min and its relation

with DO (1), the previous condition becomes

$$V_{CF} \geq VImax\frac{2}{2-Do} \quad (5)$$

Fig. 4 shows the minimum value of the capacitor CF voltage VC F as function of DO when considering the maximum input voltage 250 V_{rms} (worst case).

It is important to consider a parameter p_{CF} that defines the excess voltage of the capacitor C_F (related to its minimum value V_{CF} min). This margin introduces a restriction in the design of the converter, namely, in the maximum value of the input inductances, as will be further analyzed. Considering this, the V_{CF} voltage will be defined by

$$V_{CF} = V_{CF\,min}(p_{CF} + 1) \text{ with } p_{CF} > 0. \quad (6)$$

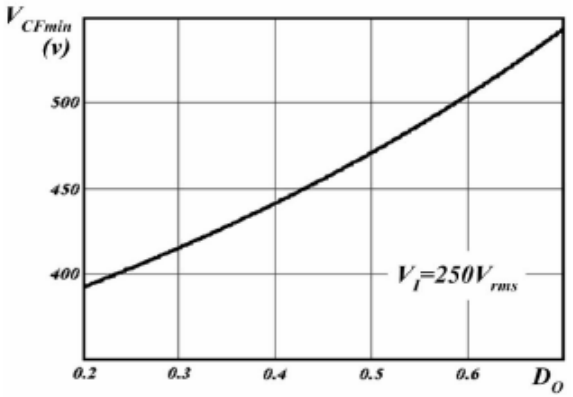

Fig.4. $V_{CF\,min}$ as function of DO for an input V_{rms} voltage of 250 V_{rms}.

III. MINIMUM INPUT POWER

During the CCM operation of the output filter, the output duty ratio D_O is constant, meaning that the input boosts have a minimum input duty ratio, i.e., $D_{I\,min} = D_O/2$. Considering the value of $D_{I\,min}$ and the value of the input inductances L, the converter imposes a minimum input power PI m in. This minimum input power must be suppressed to avoid the increase of V_{CF} voltage to uncontrollable values. This problem was solved in [24]–[27] by using a half-controlled input rectifier, with a random control, which disconnects the converter from the mains if the capacitor voltage V_{CF} stays out of control. With this circuit, it is possible to operate the output filter in CCM for very low loads and operate with no load. However, simpler and cheaper, a bridge diode can be used, as occurs in the topologies presented in [19]–[24], if the output inductance L_O is designed considering the correct boundary between the CCM and the discontinuous conduction mode (DCM), which guarantees the D_O reduction with low loads. Note that the D_O reduction implies the reduction of the minimum input power. This technique is also used in the proposed topology. This fact constrains the output inductance L_O, which must guarantee the correct boundary between the CCM and the DCM to operate with low loads.

In this section, the analysis of the converter with the output filter working in DCM is evaluated. In this case, the output duty ratio is not constant, and will be denoted by d_O in order to distinguish it from its constant value, when operating in CCM, D_O.

The minimum input current evolution is obtained when the boost converters operate constantly with an input duty ratio $D_I = D_{I\,min}$. For this mode of operation, the input current will be zero until the mains voltage becomes higher than $V_{CF}/2$. Fig. 9 shows the typical inductor current evolution for this operation mode and respective states for $v_I > 0$.

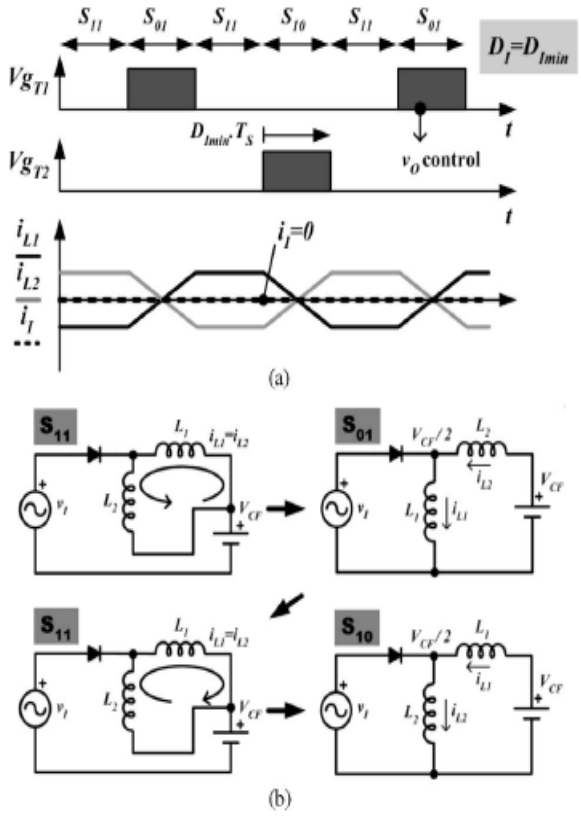

Fig. 5. Constant operation of the two low-side boosts with $D_I = D_{I\,min}$: (a) gate signals of T_1 and T_2 and inductors current waveforms; (b) equivalent circuits used to present the converter states.

For $v_I > V_{CF}/2$, the average input current $(i_I)_{TS}$ presents a low evolution, which is given by

$$\langle i_I \rangle_{TS} = \frac{V_I \sin(\omega t) - V_{CF}/2}{2L} d_O^2 T_{SO} \frac{V_{CF}}{V_{CF} - V_I \sin(\omega t)}. \quad (10)$$

For very low loads, the output duty ratio tends to zero ($P_O \to 0 \Rightarrow d_O \to 0$). This fact results in deficient commutation of the inverter transistors due to the reduced duration of t_{01} and t_{10}. To solve this problem, two solutions can be used: either using an

additional output resistance RL m ax to assure a minimum output power $P_{O\,min}$ (switched only when the output power is very low) or using an output voltage controller that allows operation in pulse frequency modulation (PFM) for low loads. In the

PFM operation, a minimum conduction time, t01m in = $t_{10\,min}$, is defined to be constant. Therefore, the output duty ratio is changed considering the increase of the time periods t_{00} or t_{11}, resulting this in a variable frequency process. For demonstration purposes of the new topology operation and explanation of the concepts introduced, the first method was adopted. The $P_{O\,min}$ selection, to avoid very short duration of the time intervals t_{01} and t_{10}, is obtained considering the analysis of the output filter in DCM.

IV. SIMULATION RESULTS

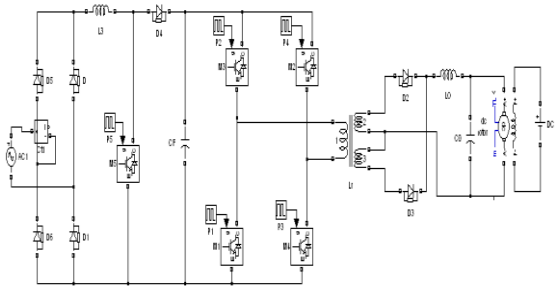

Fig.6. conventional two-stage topology

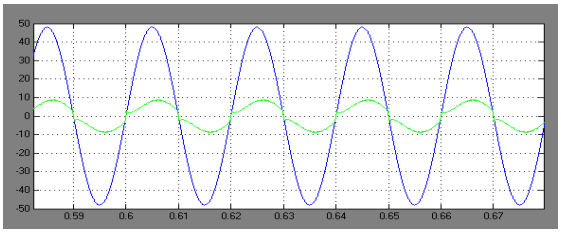

Fig.7. input voltage and currents

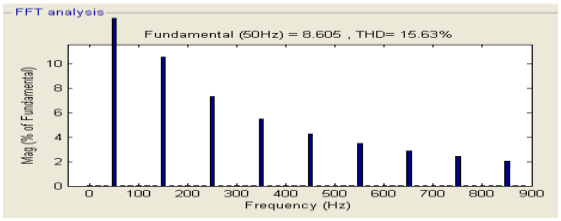

Fig.8. THD for the conventional topology

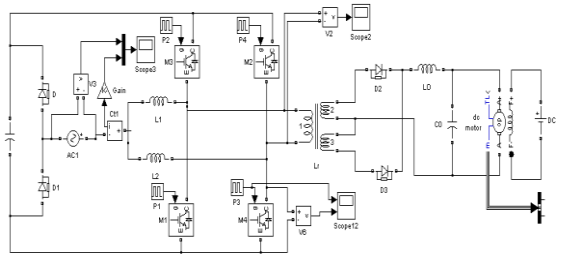

Fig.9. Proposed single-stage topology

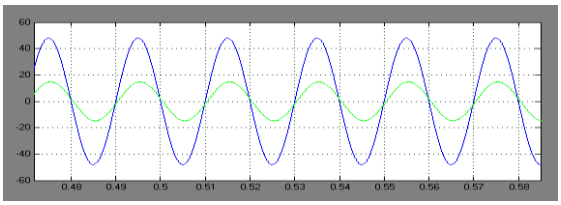

Fig.10. input voltage and currents

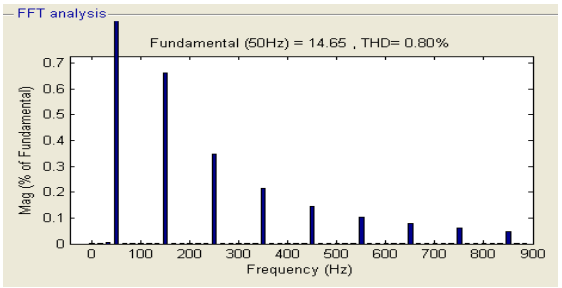

Fig.11. THD for the conventional topology

V. CONCLUSION

This paper presents a detailed analysis and design of an optimized, single-stage, single-phase full-bridge topology. Appropriate control allows for the operation of the isolated full-bridge converter in order to attain four parallel input boost converters to accomplish the PFC function with low THD. These boost converters distribute the input power uniformly by the four-inverter transistors, thereby improving the efficiency and reducing current stress. Furthermore, the topology only uses two input rectifier diodes, which also reduce the converter cost and improves the efficiency, due to the reduced number of diodes in series for each boost state. Another positive feature of this topology is related to the input current switching frequency, which is the double of the bridge transistors switching frequency, reducing the input current ripple. A full analysis of the converter operation that permits to establish design criteria that lead to simple design equations was described. The principal drawbacks are related with low power operation: 1) the existence of the two input inductors may turn this converter not suitable for low power applications due to cost and 2) for very low power operation, a

PFM control process or an additional resistance will be needed.

A 650-W prototype was built in order to obtain experimental results to validate the theoretical analysis, the adopted designed criteria, and the converter performance. The converter presented high efficiency at full load, 94%. Considering the circuit optimization, the efficiency at low power can be improved by increasing the transformer magnetizing inductor (which reduces the magnetic losses and switching losses) and also by optimizing the circuit layout (with the consequent reduction of the dissipated power in the snubber circuits). From the results presented, it is also concluded that, when comparing the proposed converter with an equivalent two-stages converter, each stage should present efficiency higher than 97%, in order to present the same efficiency as the proposed converter, at full power. This may result in an attractive converter for the industry.

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC–DC converters," IEEE Trans. Ind. Electron., vol. 50, no.5, pp. 962–981, Oct. 2003.

[2] E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Buck-boost-type unity power factor rectifier with extended voltage conversion ratio," IEEE Trans. Power Electron., vol. 55, no. 3, pp. 1123–1132, Mar.2008.

[3] M. M. Jovanovi´ and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications—An overview," IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 701–708, Jun. 2005.

[4] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC Boost rectifiers," IEEE Trans. Power Electron., vol. 23,no. 3, pp. 1381–1390, May 2008.

[5] Y. Jang and M. M. Jovanovi´, "A bridgeless PFC boost rectifier with optimized magnetic utilization," IEEE Trans. Power Electron., vol. 24, no. 1, pp. 85–93, Jan. 2009.

[6] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "A novel bridgeless buck-boost PFC converter," in Proc. IEEE Power Electron. Spec. Conf., 2008, pp. 1304–1308.

[7] W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, "Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction," IET Power Electron., vol. 1, no. 2, pp. 194–202, Jun. 2008.

[8] R. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in Proc. IEEE Power Electron. Spec. Conf. (PESC), 1994, pp. 1137–1144.

[9] R. Redl and L. Balogh, "Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage," in Proc. IEEE Appl. Power Electron. Conf. (APEC), 1995, pp. 454–458.

[10] C. Qiao and K. Ma Smedley, "A topology survey of single- stage power factor corrector with a boost type input-current-shaper," IEEE Trans. Power Electron., vol. 16, no. 3, pp. 360–368, May 2001.

[11] O. Garcia, J. A. Cobos, P. Alou, R. Prieto, and J. Uceda, "A simple single-switch single-stage ac/dc converter with fast output voltage regulation," IEEE Trans. Power Electron., vol. 17, no. 2, pp. 163–161, Mar. 2002.

[12] Q. Zhao, F. C. Lee, and F.-s. Tsai, "Voltage and current stress reduction in single-stage power factor correction AC/DC converters with bulk capacitor voltage feedback," IEEE Trans. Power Electron., vol. 17, no. 4, pp. 477– 484, Jul. 2002.

[13] S. Luo, W. Qiu, W. Wu, and I. Batarseh, "Flyboost power factor correction cell and a new family of single-stage AC/DC converters," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 25–34, Jan. 2005.

[14] H.-F. Liu and L.-K. Chang, "Flexible and low cost design for a flyback AC/DC converter with harmonic current correction," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 17–24, Jan. 2005.

[15] J.-Y. Lee, "Single-stage AC/DC converter with input-current dead-zone control for wide input voltage ranges," IEEE Trans. Power Electron., vol. 54, no. 2, pp. 724–732, Apr. 2007.

[16] D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica, "A single-stage AC/DC converter with high power factor, regulated bus voltage, and output voltage," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 218–228, Jan. 2008.

[17] A. L´ zaro, A. Barrado, M. Sanz, V. Salas, and E. Ol´as, "New power factor correction ac–dc converter with reduced storage capacitor voltage," IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 384–397, Feb.2008.

[18] J. Zhang, M. M. Jovanovic, and F. C. Lee, "Comparison between CCM single-stage and two-stage boost PFC converters," in Proc Appl. Power Electron. Conf. Expo. (APEC), 1999, vol. 1, pp. 335–341.

[19] M. Qiu, G. Moschopoulos, H. Pinheiro, and P. Jain, "Analysis and design of a single stage power factor corrected full-bridge converter," in Proc. IEEE Appl. Power Electron. Conf., 1999, pp. 119–125.
[20] S. Li and G. Moschopoulos, "A simple AC–DC PWM full-bridge converter with auxiliary transformer winding," in Proc. IEEE Int. Telecommun. Energy Conf. (INTELEC), 2003, pp. 216–223.
[21] G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor corrected converter topologies," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 23–35, Feb. 2005.
[22] L. Rosseto and S. Buso, "Single-phase AC/DC integrated PWM converter," in Proc. Int. Telecommun. Energy Conf. (INTELEC), 2000, pp. 411–418.
[23] L. Rosseto and S. Buso, "Digitally-controlled single-phase AC/DC integrated PWM converter," in Proc. IEEE Ind. Appl. Soc. Conf. (IAS 2001), Oct., pp. 2159–2156.
[24] L. Rosseto and S. Buso, "Digitally-controlled single-phase single-stage AC/DC PWM converter," IEEE Trans. Power Electron., vol. 18, no. 1,pp. 326–333, Jan. 2003.
[25] V. Anunciada and R. D. Monteiro, "Single stage full-bridge converter with power factor correction," in Proc. IEEE Power Electron. Spec. Conf., 2001, pp. 1566–1570.
[26] V. Anunciada and H. Ribeiro, "Single stage AC/DC converter with input power factor correction," in Proc. IEEE Ind. Electron. Conf. (IECON), 2003, pp. 2933–2938.
[27] V. Anunciada and H. Ribeiro, "Single stage AC/DC converter with input power factor correction," in Proc. Power Electron. Drives Syst. Conf. (PEDS), 2003, pp. 1480–1485.
[28] V. Anunciada and B. Borges, "Power factor correction in single phase AC–DC conversion: Control circuits for performance Optimization," in Proc. IEEE Power Electron. Spec. Conf. (PESC), 2004, pp. 3775–3779.