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Design & Implementation of Digital down Converter for Wcdma System

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Abstract:- In this paper, Digital Down Converter (DDC) for Wideband Code Division Multiple Access (WCDMA) signals is designed. WCDMA is a 3rd generation technology for mobile communication. The DDC shall be designed in MATLAB. The proposed DDC design consists of a WCDMA source, AWGN channel and data rate conversion system. Decimation system consists of Halfband decimation Filter and Root Raised Cosine (RRC) decimation/pulse shaping filter.The results shows a signal of sampling frequency 61.44 Msps is down converted to a sampling frequency of 7.68 Msps. Chain of two Halfband decimation filters of decimation factor 2 each and RRC decimation filter of decimation factor 2 is designed. Overall decimation factor of 8 is obtained by cascaded chain of decimation filters. Output response of designed DDC is observed. EVM and SNR parameter values are obtained and compared.

Keywords:- Numerically Controlled Oscillator (NCO), Digital down converter (DDC), Finite Impulse Response filter(FIR) , Wideband Code Division Multiple Access (WCDMA), Root Raised Cosine(RRC) , Halfband Filters, Intermediate Frequency (IF).

I. INTRODUCTION

DDC is an important component of a digital radio. It performs frequency translation to convert the high input sample rate down to a lower sample rate for efficient processing. Conventional DDC accepts a bandpass signal and performs the following operations:

- Digital mixing or down conversion of the input signal using a Numerically Controlled Oscillator (NCO) and a mixer.
- Narrowband low-pass filtering and decimation using a filter chain of halfband and RRC filters .Gain adjustment and final re-sampling of the data stream.

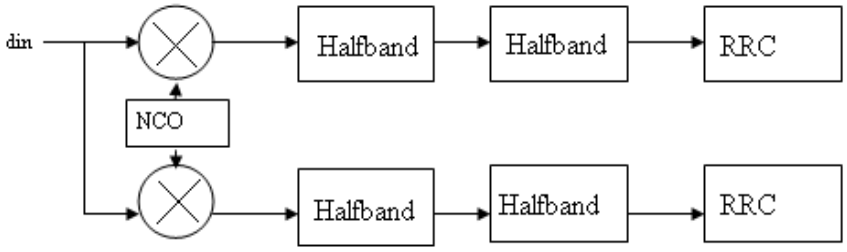

Fig 1: Basic Digital Down Converter

II. SYSTEM REQUIREMENTS

DDC must be designed to satisfy the 3rd generation partnership project (3GPP) specification which defines the transmission and reception required for base station radio of WCDMA.

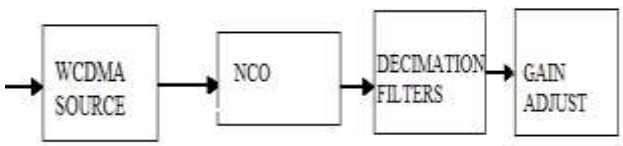

Fig 2: WCDMA System With Decimation Process

DDC is integral part of a communication system, which are used to convert the sample rate of the signal. Digital down conversion is required when a signal is converted from IF band to baseband. In addition to

sampling rate conversion, DDCs typically include frequency shifting using mixers. DDC depends mainly on the conversion ratio. For WCDMA systems, the conversion ratio is typically in the order of 8. DDC for WCDMA standard with decimation factor of 8 is designed. Fig 1 shows the top level block diagram of WCDMA. The WCDMA specification for uplink receiver path is given in Table 1.

Table 1. Specification for uplink receiver path[1]

Parameters	Values
Input signal quantization	14 bits
Output signal quantization	16 bits I & Q
Mixer properties	Tunability: Variabile
IF sample rate	61.44 MCPS
No. of carriers	1
Carrier bandwidth	5 Mhz
DDC output rate	7.68 MSPS

III. DDC DESIGN

The DDC translates one or more intermediate IF channels from a set of specified centre frequencies to 0 Hz. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR).

In signal processing, down sampling is the process of reducing the sampling rate of a signal. This is usually done to reduce the data rate or the size of the data. The down sampling factor is usually an integer or a rational fraction greater than unity. This factor multiplies the sampling time or, equivalently, divides the sampling rate. Since down sampling reduces the sampling rate, it is usually a good idea to make sure the Nyquist–Shannon sampling theorem criterion is maintained relative to the new lower sample rate, to avoid aliasing in the resulting digital signal. To ensure that the sampling theorem is satisfied, or approximately so, a low-pass filter is used as an anti-aliasing filter to reduce the bandwidth of the signal before the signal is downsampled; the overall process (low-pass filter, then down sample) is also called decimation. Fig 4 shows basic decimation process

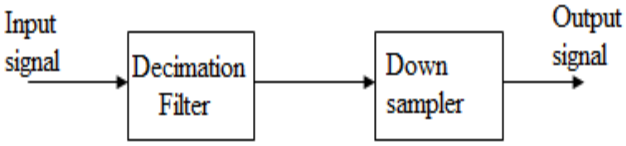

Fig 3 Decimation Process

IV. DDC FILTER DESIGN

The decimators in the DDC need to down sample the IF data from 61.44 MHz back to chip rate. The factor of 61.44/7.68 = 8 can be partitioned in a couple of ways. The channel filter is the last component of the decimation chain. Down sampling by eight at once will most likely result in an extremely long filter length and result in an inefficient hardware implementation. Additionally, RRC shaping filter allows the remaining stages to be implemented as two halfband filters, which are advantageous because half of the coefficients are zero. Instead, it was designed as a decimator with a rate of 2. The down-sample-by-4 task can be done by two stages of halfband filters with decimation rate of 2 each. FDATool is used to design multirate decimation filters and to observe the filter responses. Figure 3.2 shows the WCDMA DDC filter architecture with two halband filters and one RRC filter at the end.

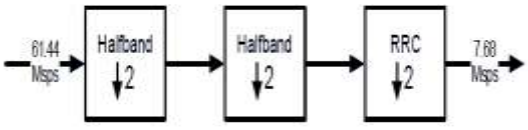

Fig 4 WCDMA DDC Filter Design
Fig shows Matlab model design of WCDMA DDC.

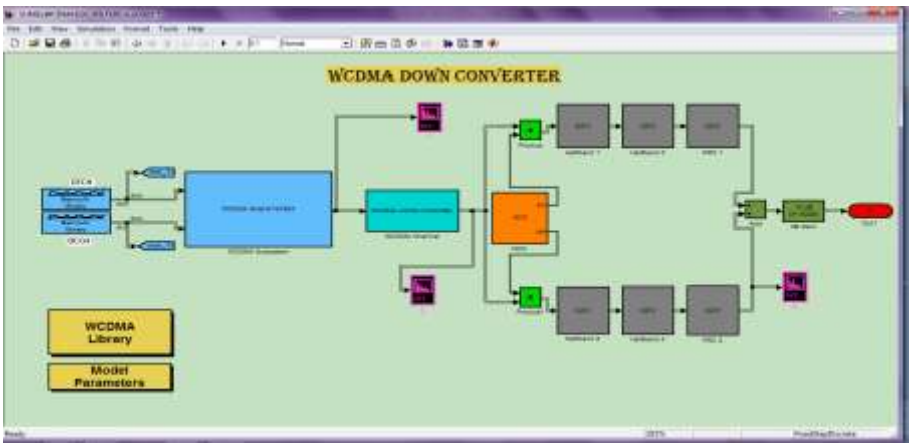

Fig 4 Matlab Model Design Of DDC.

IV. RESULTS

The DDC is designed using Matlab. The following results are concluded.

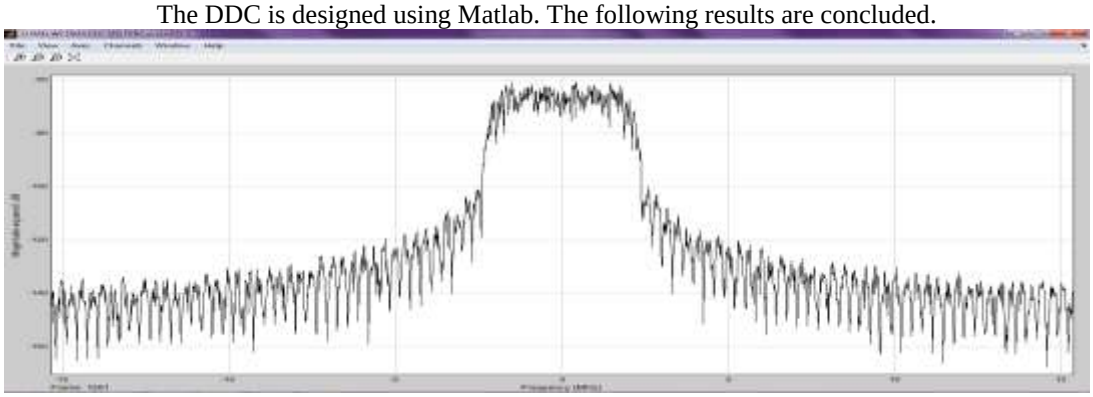

Fig 5 Input signal

The input DDC is shown in fig 5.The input DDC is a 1 carrier WCDMA composite signal whose bandwidth is of 5 Mhz.

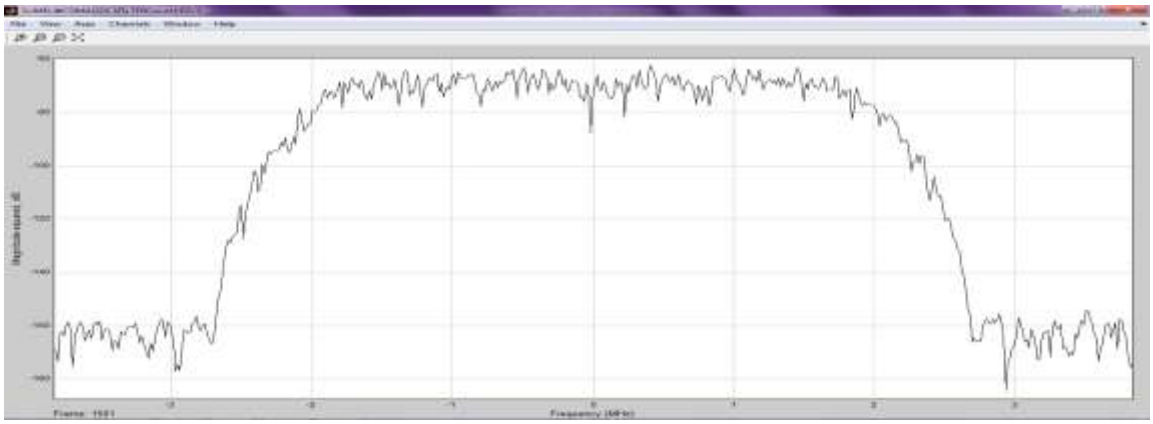

Fig 6 Output of DDC

This plot estimates the power consumption with the frequency. The power consumption has been estimated in terms of db and the frequency has been estimated in terms of MHz.

V. CONCLUSIONS

WCDMA is a rapidly growing wireless communication system that can provide broadband access with large coverage area. In the present work an effort is made to reduce the complexity of WCDMA system. From the study of literature related to WCDMA systems, it is concluded that DDC is the integral part of a WCDMA system. Study also shows that decimator filters are major part of DDC.

As higher bandwidth can lead to more data rate and also design of digital systems at large bandwidth is of great challenge. So, in these thesis decimator stages of WCDMA DDC is designed for 5 MHz bandwidth.

According to WCDMA standards, for 5 MHz channel bandwidth, DDC need to be designed for decimation factor of 8, and during their design, the spectral emission standards should be strictly followed. Decimation filtering focus mainly on suppression of 'aliasing' & reduction of the received noise. The signal-to-noise ratio is hence improved by filtering. The Calculated EVM for DDC is 18.28%, which translates to 14.34 dB of SNR before de-spreading. The SNR is around 40 dB.

IV. SCOPE FOR FUTURE WORK

For designing a multistage DDC, the development of a reliable method to find the number of optimum number of stagesmay be future area of concern. In addition to design of individual stages of decimator, future work may be on the design of efficient direct digital synthesizer and mixer also. The work done in this thesis may be extended for other broadband communication systems.

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