

## Low Power, Area and Delay Efficient Carry Select Adder Using Bec-1 Converter

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**Abstract:-** In performing fast arithmetic functions, Carry select adder (CSLA) is one of used in many data processing processors to perform fast arithmetic functions. Adders are the basic building blocks in digital integrated circuit based designs. Ripple carry adders are slowest adders as every full adder must wait till the carry is generated from previous full adder. CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area, power and delay as compared with the regular SQRT CSLA. This work evaluates the performance of the proposed designs in terms of delay, area, power. The result analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

**Keywords:-** ASIC, Power, area and delay efficient, BEC,CSLA.

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### I. INTRODUCTION

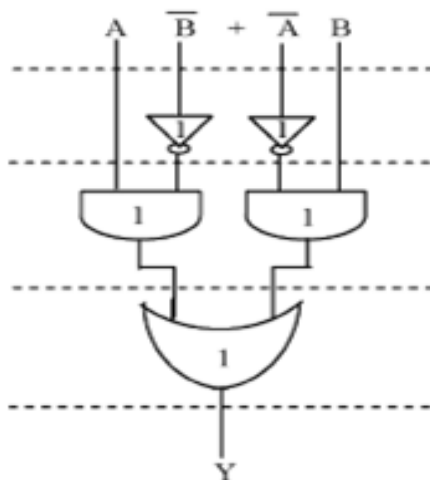
In VLSI system design the design of area and power efficient high speed logic systems are most essential. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many systems to overcome the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. But the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input  $c_{in} = 0$  and  $c_{in}=1$ , then the multiplexers are used to get final sum and carry are used.

The Binary to Excess-1 converter (BEC) is used instead of RCA with  $C_{in} = 1$  in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than Full Adder (FA) structure.

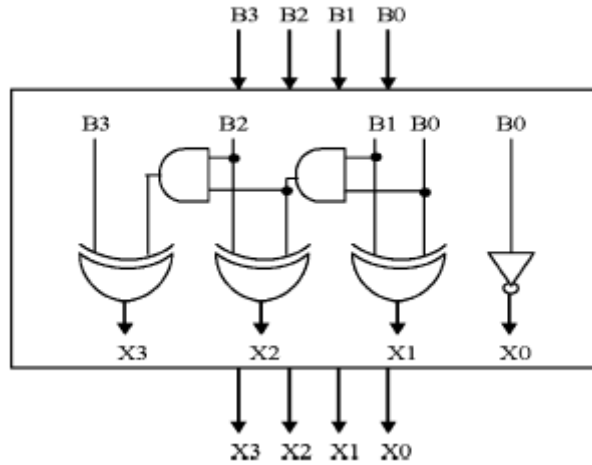
### II. CALCULATION OF DELAY AND AREA OF THE BASIC ADDER BLOCKS

The AND, OR and INVERTER (AOI) implementation of XOR gate is shown in fig.1. The operations of gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay.



**Fig1 :** delay and area

**Fig 2:** 4 bit BEC evaluation of XOR gate



Contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and INVERTER, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

### III. BINARY TO EXCESS-1 CONVERTER

To reduce the area and power consumption Binary Excess-1 converter instead of RCA with  $C_{in} = 1$ . This is the main concept of the paper, so as to reduce delay compared to regular SQR CSLA. To replace the n-bit RCA, an n+1 bit BEC is required. A structured and the function table of a 4-b BEC are shown in fig 2 and table II, respectively.

Fig3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as its input (B3,B2,B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal  $c_{in}$ . The Boolean expressions of the 4-bit BEC is listed as

$$\begin{aligned} X_0 &= \sim B_0 \\ X_1 &= B_0 \wedge B_1 \\ X_2 &= B_2 \wedge (B_0 \& B_1) \\ X_3 &= B_3 \wedge (B_0 \& B_1 \& B_2) \end{aligned}$$

**Table1** delay and area count of the basic blocks of CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

### IV. DELAY AND AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQR CSLA

The structure of the 16-b regular SQR CSLA is shown in fig 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in fig 6, in which the numerical specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

1) The group2 [in fig 6(a)] has two sets of 2- b RCA ,based on the consideration of delay values of table I. the arrival time of selection input  $c_1$  [time(t) = 7] of 6:3 mux is earlier than  $s_3$ [t = 8] and later than  $s_2$ [t = 6]. Thus,  $sum_3$ [t = 11] is summation  $S_3$  and mux[t = 3] and  $sum_2$ [t = 10] is summation of  $c_1$  and mux.

2) Other than group2, the arrival time of mux selection input is always greater than the RCA's. thus the delay of group3 to group5 is determined , respectively as follows: arrival time of data outputs from the { $c_6$ ,  $sum[6 : 4]$ } =  $c_3$ [t = 10] + mux  
{ $c_{10}$ ,  $sum[10:7]$ } =  $c_6$ [t= 13] + mux

$$\{cout, sum[15:11]\} = c10[t=16] + mux$$

3) The one set of 2-b RCA in group2 has 2 FA for  $C_{in}$  and the other set has 1 FA and 1HA for  $C_{in} = 0$ . Based on the area count of table I, total number of gate counts in group2 of table I, the total number of gate counts in group2 is determined as follows:

$$\begin{aligned} \text{Gate count} &= 57 \text{ (FA + HA + MUX)} \\ \text{FA} &= 39(3*13) \\ \text{HA} &= 6(1*6) \\ \text{Mux} &= 12(3*4) \end{aligned}$$

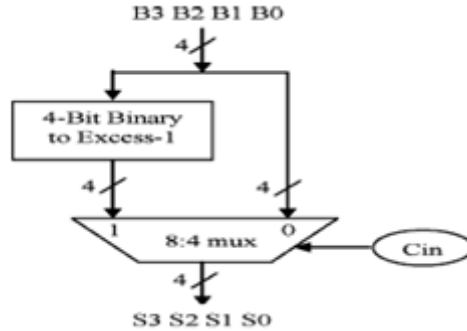


Fig.3: 4 bit BEC with 8:4 mux

Table 2 function table of 4 b BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
...	...
1110	1111
1111	0000

Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in table3.

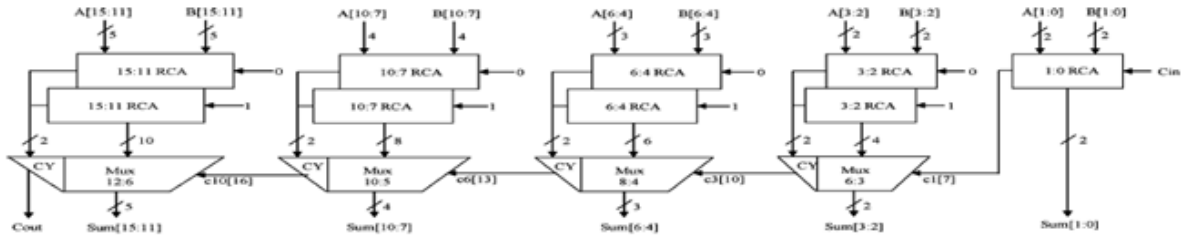


Fig 4: REGULAR 16 bit SQRT CSLA

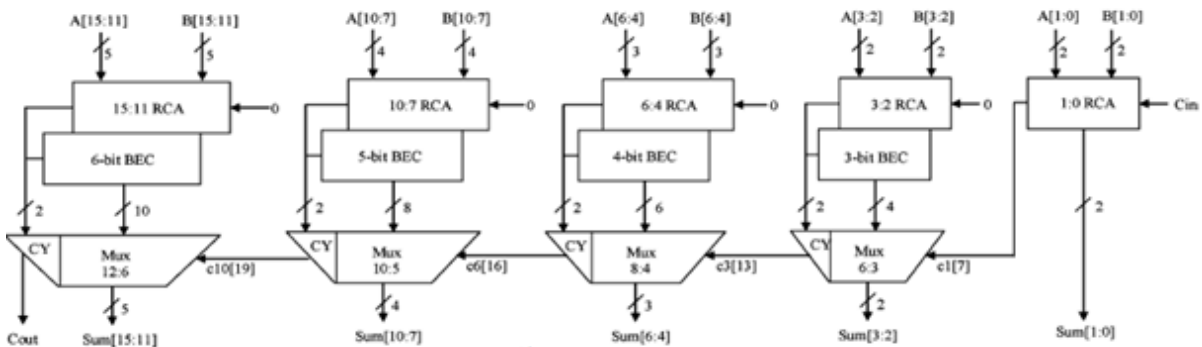


Fig 5: PROPOSED 16 bit SQRT CSLA

**Table 3** Delay and Area count of REGULAR SQRT CSLA Groups

Groups	Delay	Area
Group1	7	26
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

**Table 4** Delay and Area count of PROPOSED SQRT CSLA Groups

Groups	Delay	Area
Group1	7	26
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

## V. METHOD PROPOSED FOR 16 BIT CSLA BASED ON THE BEC-1 CONVERTER

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with  $C_{in} = 1$  to optimize the area and power is shown in fig 5. We again split the structures into five groups. Tdelay and area evaluation of each group are shown in fig 7.

1) The group2 [in fig 7(a) has one 2-b RCA which has 1FA and 1HA for  $c_{in} = 0$ . Instead of another 2-b RCA with  $c_{in} = 1$  a 3-b BEC is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of table 1, the arrival time of selection input  $c1[t = 7]$  of 6:3 mux is earlier than the  $s3[t = 9]$  and  $c3[t = 10]$  and later than the  $s2[t = 4]$ . Thus, the sum3 and final  $c3[t = 10]$  and later than the  $s2[t = 4]$ . Thus, the sum3 and final  $c3$ (output from mux) are depending on  $s3$  and mux and partial  $c3$ (input to mux) and mux, respectively. The sum2 depends on  $c1$  and mux.

FA = 13(1 \* 13) inputs from the BEC's. thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

For the remaining groups the arrival time of mux selection input is always greater than the arrival time of data

2) The area count of group2 is determined as follows:

$$\text{Gate cont} = 43(\text{FA} + \text{HA} + \text{Mux} + \text{BEC})$$

$$\text{FA} = 13(1 * 13)$$

$$\text{HA} = 6(1 * 6)$$

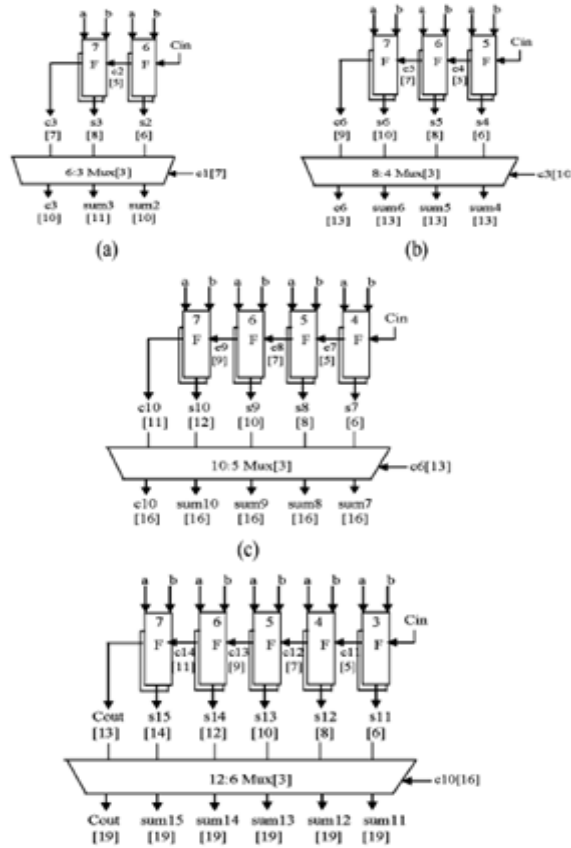
$$\text{AND} = 1$$

$$\text{XOR} = 10(2 * 5)$$

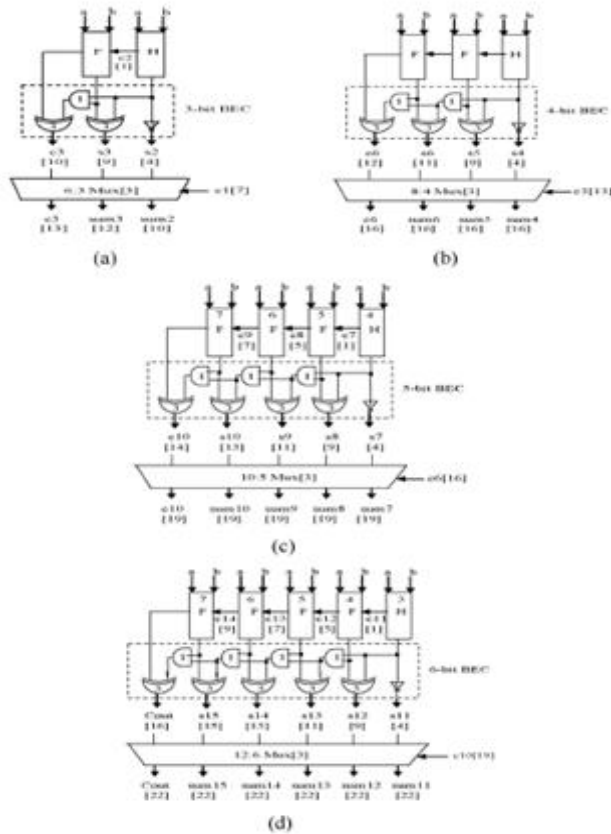
$$\text{Mux} = 12(3 * 4)$$

$$\text{NOT} = 1$$

3) Similarly, the estimated maximum delay and area of the other groups of the PROPOSED SQRT CSLA are evaluated and listed in table 4. Comparing tables 3 and 4, it is clear that the proposed system is better in delay and area, simultaneously in power.



**Fig 6** Delay and area evaluation of REGULAR SQRT CSLA:  
 (a)group2, (b)group3, (c)group4 and (d)group5



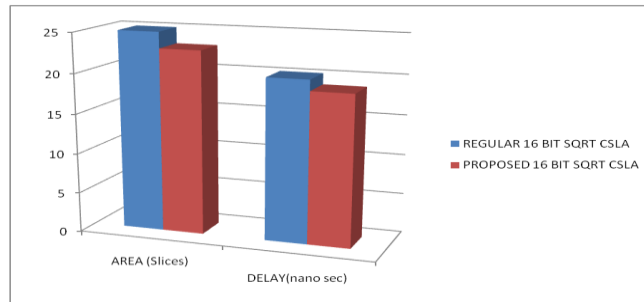


Fig 7 Delay and area evaluation of PROPOSED Sqrt CSLA REGULAR and PROPOSED Sqrt CSLA in (a)group 2, (b)group3, (c)group4, (d)group5

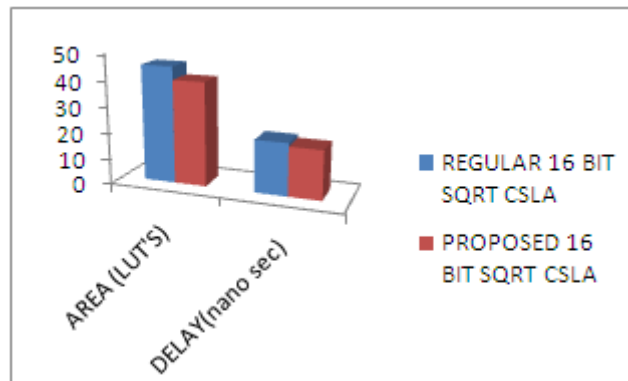


Fig 8 : Graphical charts representing area

Table 3 Comparison of REGULAR and PROPOSED Sqrt CSLA

Word Size	Adder	Delay (ns)	Area (um <sup>2</sup> )	Power (uW)			Power-Delay Product(10 <sup>-15</sup> )	Area-Delay Product(10 <sup>-21</sup> )
				Leakage Power	Switching power	Total power*		
8-bit	Regular CSLA	1.719	991	0.007	101.9	203.9	350.5	1703.5
	Modified CSLA	1.958	895	0.006	94.2	188.4	368.8	1752.4
16-bit	Regular CSLA	2.775	2272	0.017	263.7	527.5	1463.8	6304.8
	Modified CSLA	3.048	1929	0.013	235.9	471.8	1438.0	5879.6
32-bit	Regular CSLA	5.137	4783	0.036	563.6	1127.3	5790.9	24570.2
	Modified CSLA	5.482	3985	0.027	484.9	969.9	5316.9	21845.7
64-bit	Regular CSLA	9.174	9916	0.075	1212.4	2425.0	22246.9	90969.3
	Modified CSLA	9.519	8183	0.057	1025.0	2050.1	19514.9	77893.9

## VII SIMULATION RESULTS

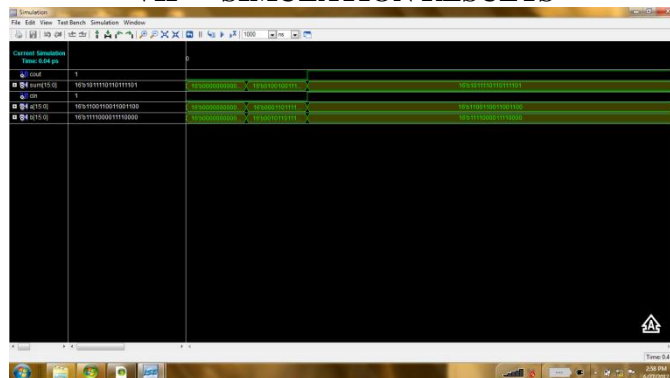


Fig 9 simulation result for REGULAR 16 b Sqrt CSLA

### VIII. CONCLUSION

When the comparison between the SQR T CSLA and modified SQR T CSLA is considered, there is the difference in simple approach is proposed in this paper to reduce the area, delay and power of SQR T CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area, delay and also the total power. The compared results show that the proposed SQR T CSLA has delay, area and power are significantly reduced.

Area and delay values of REGULAR SQR T CSLA and PROPOSED SQR T CSLA are given below, which are evaluated based on the Xilinx program of REGULAR SQR T and PROPOSED SQR T CSLA.

#### 1) Area of REGULAR SQR T CSLA

Number of Slices : 25 out of 4656 2%  
 Number of 4 input LUTs : 45 out of 9312 2%  
 Number of IOs : 50  
 Number of bonded IOBs : 50 out of 232 21%  
 Delay of SQR T CSLA is 20.215ns

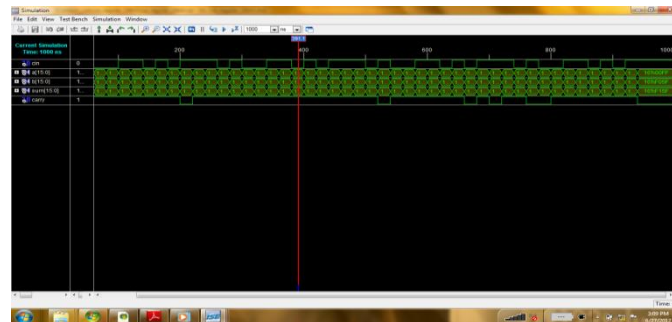


Fig 10 simulation result for PROPOSED 16 b SQR T CSLA

#### 2) Area of PROPOSED SQR T CSLA

Number of Slices : 23 out of 4656 2%  
 Number of 4 input LUTs : 40 out of 9312 2%  
 Number of IOs : 50  
 Number of bonded IOBs : 50 out of 232 21%

Delay of MODIFIED SQR T CSLA is 18.867ns

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