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Single Phase Multilevel Inverter for AC Motor

Amrita Mariam Varghese[1], Eldhose K.A.[2], Ninu Joy[3]
[1]*P.G. Student,Mar Athanasius College of Engineering,kothamangalam,kerala*
[2,3]*Assistant. Professor, Mar Athanasius College of Engineering,kothamangalam,kerala*

Abstract:-As the demand for electrical energy is increasing, renewable energy sources has come into popularity especially photovoltaic systems (PV). PV can act as a voltage source which is feeding a power circuit. This study proposes a single phase multilevel inverter topology fed from a PV panel with a multicarrier phase disposition sinusoidal pulse width modulation scheme (PWM) for the generation of gate signals for power switches. Desired number of output levels: 3, 5, 7 and 9 is obtained by controlling modulation index. The proposed inverter configuration was subjected to an R-L load. An LC filter is modelled to obtain pure sine wave output and it's given to the load. %THD value for output current and voltage of the proposed configuration is determined. Simulation has been carried out to study the performance of the proposed topology in MATLAB/SIMULINK environment. Simulation results analysed and results presented for circuit.

Keywords:- Photovoltaic (PV), multilevel inverter, PWM, THD

I. INTRODUCTION

The ever increasing energy consumption has created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the sun's energy directly into electricity. Energy generated by photovoltaic can be delivered to drive electrical machines through inverters. Multilevel inverters has been developed due to the increase in power level of industrial applications, especially high power application. The topologies can be able to handle voltage/power in range of KV/MW. Multilevel starts with a three level inverter introduced by *Nabe*. By increasing the number of levels the output voltage has more steps generating a staircase waveform. Conventional multilevel inverters include diode clamped, flying capacitor[1], cascaded H bridge (CHB).

This paper presents a new topology of a cascaded multilevel inverter fed by a photovoltaic (PV) module that has less switches compared to the conventional topologies and has higher number of output levels. By making use of appropriate PWM techniques, a multilevel inverter with lower THD can be designed that would be useful for the design of a more compact filter. The proposed topology is similar to a CHB inverter configuration with a difference that in each H-bridge an auxiliary/clamping/bidirectional switch is provided to improve the overall harmonic profile of the output waveforms. Analysis of Operating principles and switching functions are carried out and simulation results are presented.

II. PROPOSED CIRCUIT CONFIGURATION

The block diagram of the single-phase PV fed inverter is shown in fig.1. The PV module is connected to the input of inverter as the source. The power generated by inverter is delivered to the load. A dc-dc boost converter was required because the PV arrays have a lower voltage than the single phase voltage. The LC filter is modelled to obtain pure sine – wave as output and is given to the load. Proper switching of the inverter can produce nine output voltage levels: Vs/2, Vs, 3Vs/2, 2Vs,0, -Vs/2, -Vs,-3Vs/2, -2Vs. The auxiliary switches should be properly switched depending on the direction of current.

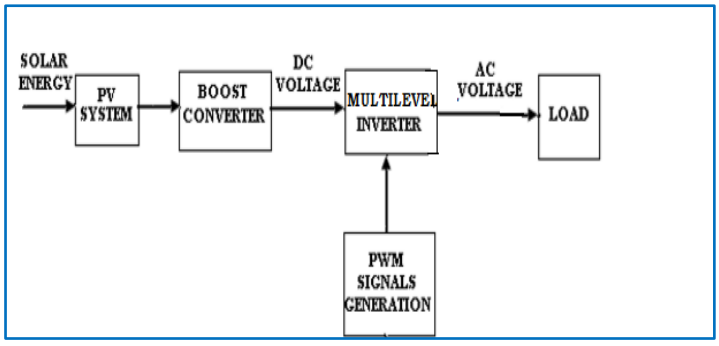


Fig.1: Block diagram of the proposed circuit

A. PV Array Model and Boost Converter

The optimum power of the PV is useful for any purposes. Due to the various level of insolation, the power output of the PV varies instantly. The overall output of PV depends on the number of cellsin the array, the total power is the contribution of each cell. So, by calculating the output of one cell, we may calculate the total output. The Fig .2 shows the equivalent circuit of a PV cell.

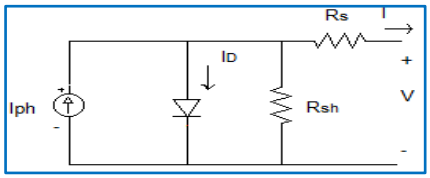


Fig.2: Equivalent circuit of a PV cell

Using equivalent circuit, the nonlinear Vpv-Ipv characteristics of PV module is:

$V_{pv} = \frac{1}{\lambda}\ln\left(\frac{Isc - Ipv + I_O}{Io}\right) - R_s I_{pv}$

Where Iscis the cell short-circuit current, Io is the reverse saturation current, Rsis the series cell resistance, and λ is a constant coefficient and depends upon the cell material. Equation expresses a nonlinear relation between voltage current characteristic of a PV module. The PV array is formed by the combination of many PV cells connected in series and parallel fashion to provide the desired value of output voltage and current. This PV array exhibits a nonlinear insolation-dependent V-I characteristic, mathematically expressed [2,3]consisting of Ns cells in series and Np cells in parallel as

$V_A = -I_A\left(\frac{N_S}{N_P}\right) + \left(\frac{N_S}{\lambda}\right)\ln\{1 + \frac{Nplph - I_o}{Nplo}\}$

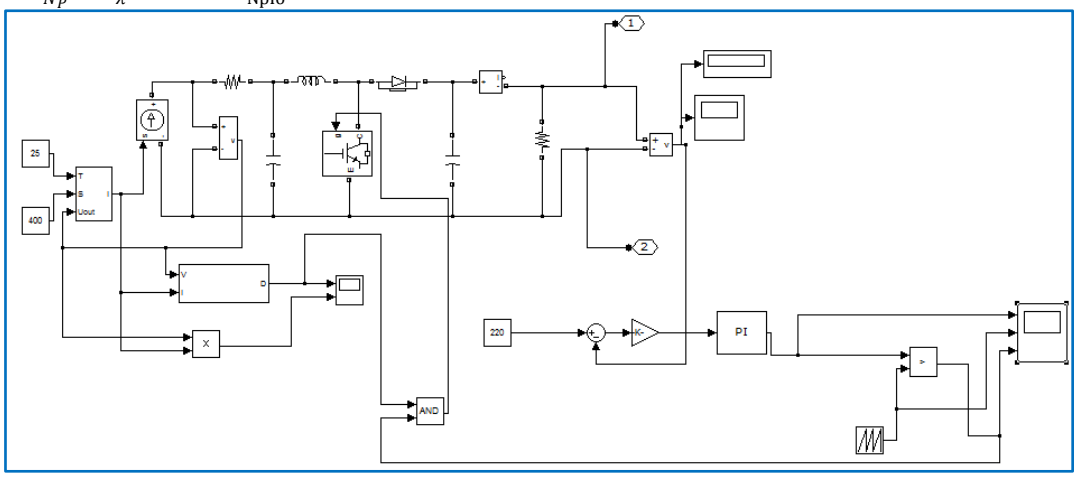


Fig.3: SIMULINK model of a PV array and Boost converter

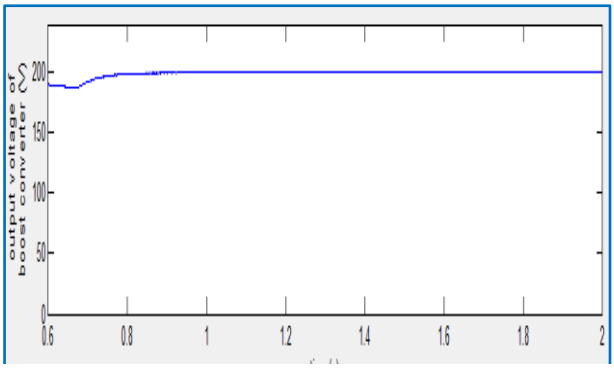


Fig.4:Input voltage to the multilevel inverter

τ = (q/AKT); q is the electric charge; A is the completion factor; K is the boltzmann's constant; T is the absolute temperature; Rs is the cell series resistance; Iph is the current; Io is the cell reverse saturation current; I_A and V_A are solar cell array current and voltage.

Boost converter is connected to the output of the PV module [4].A dc-dc boost converter is added to obtain the single phase voltage required by electric machines as the PV arrays have a lower voltage.Fig.3.shows the SIMULINK model of a PV module withboost converter and fig.4 shows the output of the above model.

B. Multilevel Inverter Topology

A single phase nine level inverter was developed from the five- level inverter [10] as shown in fig.5. It comprises of a two single phase conventional H-bridge [7.8,9], two bidirectional switches and a capacitor voltage divider formed by C_1,C_2,C_3,C_4 as shown in fig.5. High power semiconductor devices such as IGBT or GTO transistors are used as switches. Turning ON of switches permits the addition of capacitor voltages and generates high voltage at the output. For an n- level power conversion the switches need to withstand only a small fraction (normally V_s/(n-1)) of total supply voltage V_s.

The proposed inverter's operation can be divided into nine switching states [6, 12]. Switching pattern is given in table. I. The required nine levels of output voltage can be generated as follows.

Mode 1:Half of the positive output (V_S/2) is obtained. Bidirectional switch,S_a is ON, connecting the load positive terminal to voltage across C_2 and S_6 and S_2 are ON, connecting the load negative to the ground. All other controlled switches are OFF.

Mode 2:Maximum positive output (V_S) is obtained. $S_1$is ON connecting the load positive terminal to capacitors C_1 and C_2, and S_6, S_2 are ON connecting the load negative to ground. All other controlled switches are OFF.

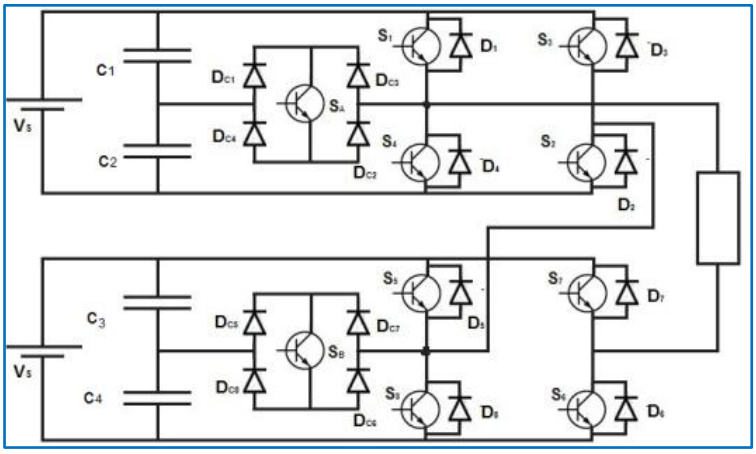


Fig. 5: Configuration of single phase nine level multilevel inverter

Mode 3:Three -half of the positive output ($3V_S$/2) is obtained. S_1, S_2, Bidirectional switch,$S_a$are ON, connecting the load positive terminal to voltage across C_1,C_2 and C_4 and $S_6$is ON, connecting the load negative ground. All other controlled switches are OFF.

Mode 4:Twice maximum positive output ($2V_S$)is obtained. S_1,S_2,$S_5$are ON connecting the load positive terminal to capacitors C_1,C_2,C_3 and C_4 and S_6 is ON connecting the load negative to capacitors ground.All other controlled switches are OFF.

Mode 5:Zero outputis obtained. This level can be produced by two switching combinations. Either switches S_2,$S_6$are ON or S_4,$S_7$are ON.All other controlled switches are OFF. The load terminals are short circuited and output is zero.

Mode 6:Half of the negative output (-V_S/2)is obtained. S_7,$S_3$are ON, connecting the load negative to capacitor C_1 and Bidirectional switch,S_a is ON, connecting the load positive terminal to ground. All other controlled switches are OFF.

Mode 7:Maximum negative output (-V_S)is obtained. S_7, $S_3$are ON, connecting the load negative terminal to capacitors C_1 and C_2, and $S_4$is ON connecting the load positive to ground.All other controlled switches are OFF.

Mode 8:Three -half of the negative output (-$3V_S$/2) is obtained. S_7,S_B,S_3 ON, connectingthe load negative terminal to voltage across C_1, C_2 and C_3 and $S_4$is ON, connecting the load positive terminal. All other controlled switches are OFF.

Mode 9:Twice maximum negative output (-$2V_S$)is obtained. S_7,S_8,$S_3$are ON, connecting the load negative terminal to capacitors C_1,C_2,C_3 and $C_4$and S_4 is ON connecting the load positive to ground.All other controlled switches are OFF.

Table 1.shows the switching combinations that generated the output voltage levels.An LC filter is designed at the load side to converter the inverter output (i.e. square wave) into pure sinusoidal wave and also to eliminate higher order harmonics.

Table I: switching pattern with corresponding output voltages

Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_a	S_b
Vs/2	0	1	0	0	0	1	0	0	1	0
Vs	1	1	0	0	0	1	0	0	0	0
3Vs/2	1	1	0	0	0	1	0	0	0	1
2Vs	1	1	0	0	1	1	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0
-Vs/2	0	0	1	0	0	0	1	0	1	0
-Vs	0	0	1	1	0	0	1	0	0	0
-3Vs/2	0	0	1	1	0	0	1	0	0	1
-2Vs	0	0	1	1	0	0	1	1	0	0

III. PWM MODULATION

In this paper a multicarrier phase disposition scheme is used to generate gate signals [5]. Gate signals are obtained by comparing sinusoidal reference or modulating signal at fundamental frequency with four triangular carrier signalat higher frequencies. Here switching frequency is adopted as 2 KHz[11] for better performance. Each of the carrier signals is compared with the rectified modulating signal, depending upon the number of levels to be obtained at the output. In the proposed circuit, switches in the first leg of each H-bridge and the auxiliary switches are switching at the rate of carrier signal frequency, whereas the remaining switches will be operating at fundamental frequency.The proposed inverter operates through eight modes.

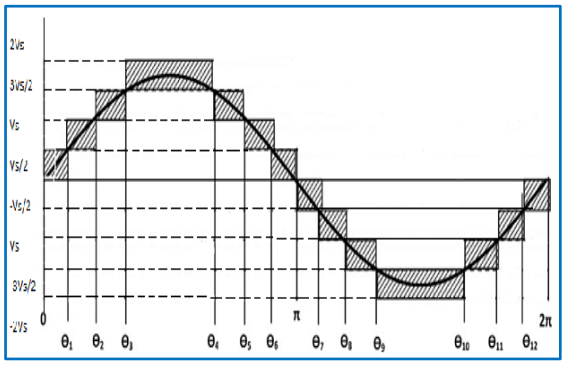


Fig.6: switching angle for each output level

Fig.6 shows the output voltage and switching angle for one cycle.The eight modes are as follows.

Mode1(vs/2) :$0<wt<\theta_1$and $\theta_6<wt<\pi$ *Mode2*(vs):$\theta_1<wt<\theta_2$and$\theta_5<wt<\theta_6$

Mode3(3vs/2):$\theta_2<wt<\theta_3$and $\theta_4<wt<\theta_5$ *Mode4*(2vs):$\theta_3<wt<\theta_4$

Mode5(-vs/2):$\pi<wt<\theta_7$and $\theta_{12}<wt<2\pi$ *Mode6*(-vs):$\theta_7<wt<\theta_8$.and$\theta_{11}<wt<\theta_{12}$

Mode7(-3vs/2):$\theta_8<wt<\theta_9$and$\theta_{10}<wt<\theta_{11}$*Mode8*(-2vs):$\theta_9<wt<\theta_{10}$

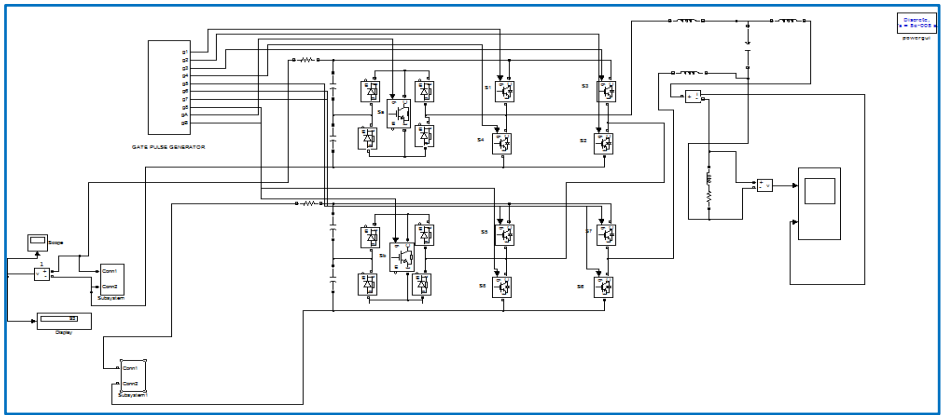


Fig.7: SIMULINK model of the proposed circuit with LC filter

Generally modulation index [14] is given by $M_a = \frac{Ac}{Am\ (k-1)}$

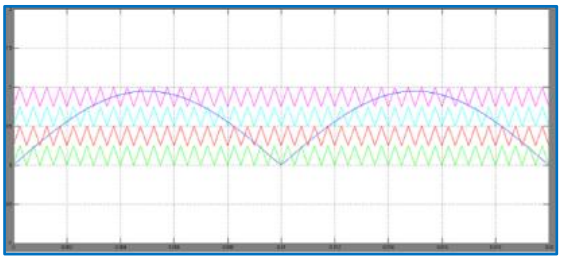
Where Ac and Amis the amplitude of the carrier signal and reference signal and *k* the number of voltage level synthesized per half-cycle. For $M_a < 0.25$, only lower carrier gets compared with reference signal and three level output is obtained if $0.25 < M_a < 0.5$, carriers T_1 and T_2 are compared and a five level output [10, 13] is obtained. A seven level output is obtained with $0.5 < M_a < 0.75$. When $M_a$value is greater than 0.75,a nine level output is obtained. The gate signals are generated by logic combination of signals generated by comparison of reference and carrier signal. Also the % THD for different output levels is shown in the Table.II.

IV. SIMULATION RESULTS

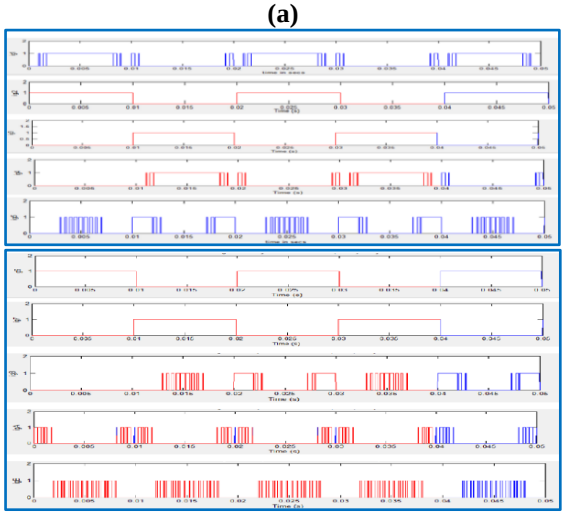
The simulation result of proposed PV fed cascaded multilevel inverter topology with and without filter has been simulated in MATLAB SIMULINK.The proposed inverter is capable of synthesizing 3-,5-,7-,9-levels. The model of the proposed circuit with filter is shown in fig.7. PWM modulation signals and gate signals for the switches S_1 to S_8, S_A and S_B for a modulation index of 0.8and simulated waveforms of output voltage and current for an input voltage of 200V (single phase voltage), R=50Ω, L =50mHfor different modulation index are obtained as seen in fig.8. The % THD was found and a very small size filter was designed to obtain a %THD of 0.31% for a nine level multilevel inverter and also for three level, five level and seven level inverter %THD was obtained as 1.88%, 1.7% and 0.4% respectively as shown in Table II.

Table.II: comparison of %THD in output waveforms

Levels	**Without Filter(%Thd)**		**With Filter(%Thd)**	
	Voltage	Current	Voltage	Current
Three Level	56.8	16.81	1.88	1.99
Five Level	38.9	12.36	1.7	1.7
Seven Level	24.16	7.46	0.40	0.41
Nine Level	16.97	5.38	0.318	0.307



(a)



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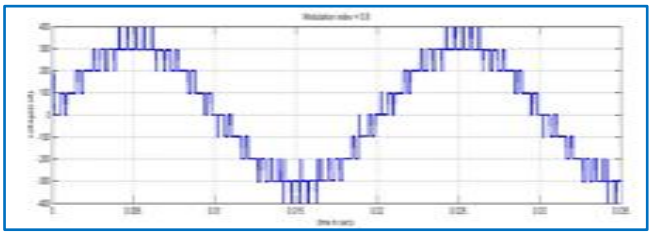

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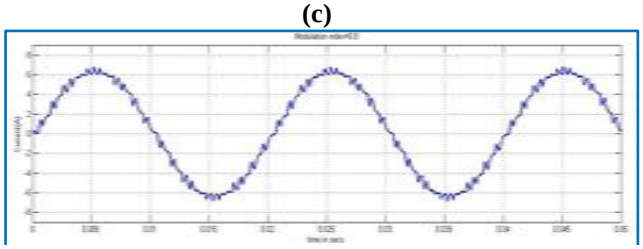

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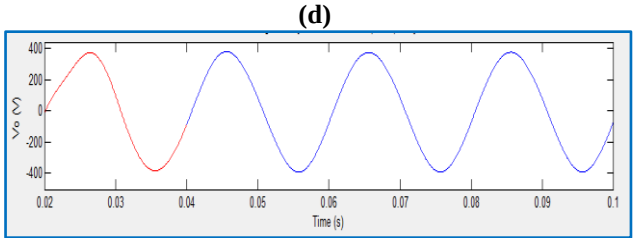

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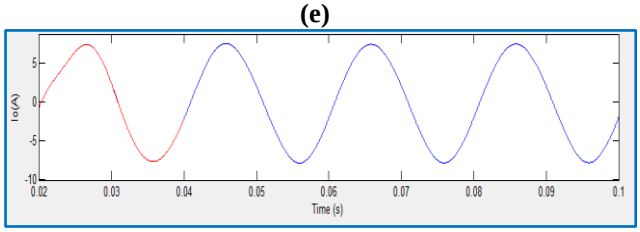

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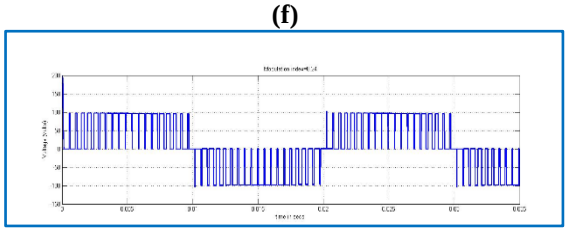

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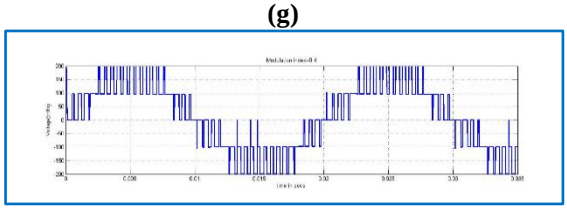

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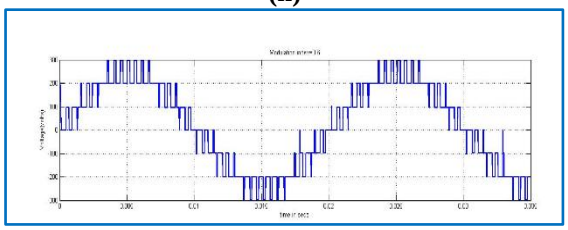

(i)

Fig.8: (a) PWM modulation signals;**(b)** Gate signals for switches S_1,S_2,S_3,S_4,S_5,S_6,S_7,S_8,S_a,S_bSimulation output for M_a =0.8(9 level):-without filter**(c)** output voltage **(d)** load current, with filter **(e)** output voltage **(f)** load current; Output voltage without filter:-**(g)**for M_a = 0.24 (3 level);**(h)**for M_a = 0.4 (5 level), **(i)**for M_a = 0.6 (7 level)

V. CONCLUSION

A configuration for multilevel cascaded inverter fed by PV that can be applied to electric drives is presented in this paper. The working, switching functions and modulation schemes have been analyzed here. The output voltage and current for circuits with and without filter have been determined. By controlling modulation index, the desired number of levels in the output has been obtained for both the former circuits. Also the % THD for each level with and without filter has been determined for each of the desired levels. The harmonics was greatly reduced to 0.31%with the design of a LC filter and a sinusoidal output at fundamental frequency was obtained.

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