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Lossy and Lossless Current-mode Integrators using CMOS Current Mirrors

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Abstract:- Analogue design has been historically viewed both in voltage-mode and current-mode dominated form of signal processing. In literature wide variety of techniques and circuits are available for the design of different current-mode signal processing circuits suitable for VLSI implementation. In this paper we present the major current-mode building blocks using complementary CMOS current-mirror pairs such as current adders and current integrators (lossy and lossless). These building blocks form the basic constitutional blocks for the implementation of second-order continuous-time current-mode active filters. All the proposed circuits presented in this paper were tested in SPICE using 0.5µm CMOS process parameters provided by MOSIS (Agilent) and the results thus obtained were in accordance with the theoretical values.

Keywords:- Complementary CMOS current-mirrors, current-adders, current-mode integrators, active filters, analog circuit design.

I. INTRODUCTION

State-of-the-art of analogue integrated circuits design is receiving tremendous boost from the development and application of current-mode processing, which is rapidly dominating traditional voltage-mode designs. Current-mode technique to signal processing has been recently receiving considerable attention, due to the fact that this technique offers one or more of the following advantages: (i) Higher slew rates (ii) Lower power consumption (iii) Higher frequency range of operation (iv) Better accuracy and (v) Improved linearity, over voltage-mode techniques. [1], [2], [8], [11] and [16]. Also, current-mode signal processing is a very attractive approach due to the simplicity in implementing operations such as addition/subtraction, multiplication by a constant, and the potential to operate at higher signal bandwidths than their voltage-mode analogues. Some of the approaches widely investigated so far are current-mode building blocks based current-mode circuits; Gm-C based current-mode circuits, switched capacitor and switched current circuits, Current-mode translinear and Log-domain circuits. All of them can be employed to devise fully integrable implementation in BiPOLAR, CMOS, and BiCMOS technology.

Although BJTs and FETs are both current output devices often the transistors are assembled into voltage oriented circuits and systems. A key performance feature of current-mode processing is inherent wide bandwidth capability, and in a current amplifier the transistor is useful almost up to its unity-gain bandwidth (f_T). Recent advances in IC technologies have meant that state-of-the-art analogue IC design is now able to exploit the potential of current-mode analogue signal processing, providing attractive and elegant solutions for many circuits and system problems.

Interest in current-mode (CM) filters has been growing due to the fact that current-mode devices have wider dynamic range, improved linearity, and extended bandwidth compared with voltage-mode devices [11]. The commonly used circuit techniques for designing current-mode filters are mainly classified into two categories.

(i) One technique is based on the transformation of the voltage-mode circuits to current-mode ones, such as the adjoint network [12], the RC: CR dual transformation [15] and the inverse-complementary network [19] etc.

(ii) The other technique uses the direct current-mode integrators as the basic cell of the design biquad [2], [6], [9] and higher-order filters [20].

II. PROPOSED CIRCUITS

Current-mode signal processing is quite attractive for low power supply voltage operation and high frequency application. In this paper design of current-mode circuits are presented using nMOS transistor current mirrors and pMOS transistor current sources as active loads. In these circuits, pMOS transistors are used for DC current sources which provide bias currents to each current mirror and also behave as active loads of the current mirror. The currents of these sources must match each other and also match with DC currents of each current

mirror to give a proper DC bias to transistors. However the matching is sometimes difficult due to the parameter mismatch between nMOS and pMOS transistors.

1) Current Adder using Current Mirrors: Figure 1 shows a multi-output current adder based on an nMOS current mirror where i_k (k = 1, 2, …, n) is the input signal current and I_B is the bias current.

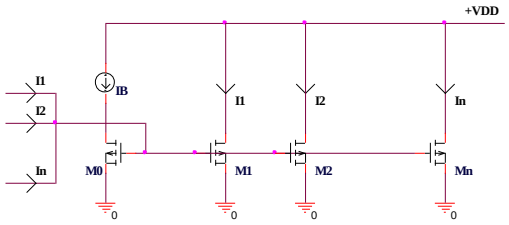

Fig. 1: Multi-Output Current Adder

Assuming, that all transistors have an equal aspect ratios (W/L), we have the output current I_k as $I_k = (I_B + i_i)$ where, $i_i = i_1 + i_2 + ... + i_n$.

2) Current Integrators using Current Mirrors

(i) Lossy Current Integrator (Non-Ideal Current Integrator): Figure 2 shows a lossy current integrator which consists of an nMOS and a pMOS current mirror.

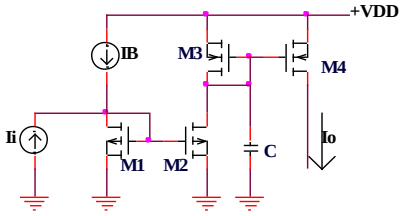

Fig. 2: Lossy Current Integrator

The given circuit can easily be extended to a multi-input and multi-output structure by adding input current sources parallel to i_i and output transistors parallel to M_4. The output current is given by $I_O = (I_B + i_i)$ where i_i is the input signal current and it is assumed that (W/L) ratios are equal. Figure 3 shows the small-signal equivalent circuit of the lossy current integrator shown in Figure 2 where R_1 and R_3 are the small-signal equivalent resistances of M_1 and M_3 respectively. From Figure 3, we can obtain the current transfer function T_I (s) as: $T_I(s) = \frac{i_o}{i_i} = \frac{g_{m2} g_{m4} R_1 R_3}{1 + sCR_3}$ where, g_{m2} and g_{m4} are respectively the transconductance of transistors M_2 and M_4. R_1 and R_3 are respectively the input resistances of transistors M_1 and M_3. Thus, we can realize a lossy current integrator which can be also be used as a first-order filter section.

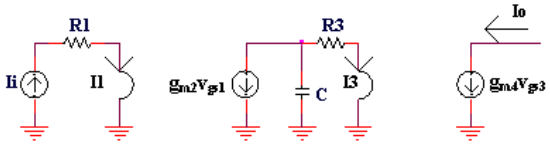

Fig. 3: AC Equivalent Circuit (Lossy Current Integrator)

The transistors M_1 and M_2 of the circuit shown in Figure 2 behaves as an input buffer and in some applications where the input buffer is not required, this section can be removed thereby simplifying the circuit as shown in Figure 4.

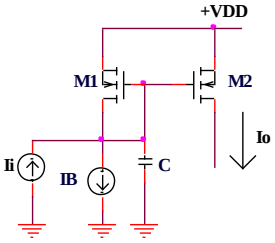

Fig. 4: Simplified Lossy Current Integrator

(ii) Lossless Current Integrator (Ideal Current Integrator): Figure 5 shows a lossless current integrator (Type-I). The transistor M_5 which provides a positive feedback is added to the lossy current integrator of Figure 2 to cancel the loss of the integrator. I_{B2} is the DC bias current source of M_5, M_6, M_7, and M_8 are also added to obtain an inverted output.

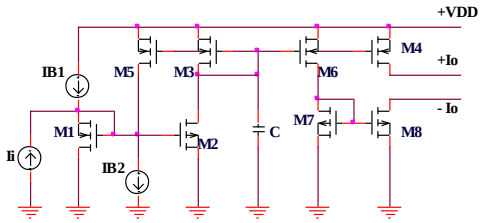

Fig. 5: Lossless Current Integrator (Type-I)

Figure 6 shows another lossless integrator structure (Type-II) in which positive feedback is provided through M_4 and M_5 to cancel the loss of the integrator. This circuit contains fewer transistors than Figure 5. Since lossless integrators have infinite gain at DC, they become unstable when they are used alone due to possible DC offset. Therefore in most applications of the integrators, such as active filters, they are generally used with negative feedback loops. The lossless integrators shown in Figures 5 and 6 contains two DC current sources I_{B1} and I_{B2}, however I_{B1} may be provided from the output DC current of a previous stage and I_{B2} can be canceled by the DC current of a negative feedback loop, thereby simplifying the structure of the circuit.

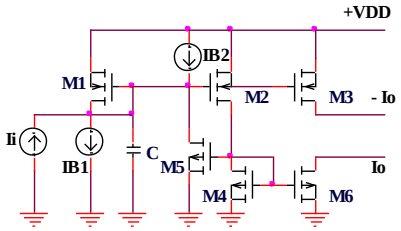

Fig. 6: Lossless Current Integrator (Type-II)

III. SIMULATION RESULTS

The workability of the proposed circuits were tested and verified in SPICE using 0.5µm CMOS process parameters provided by MOSIS (AGILENT) as listed in Table-1.

TABLE-1: CMOS PROCESS PARAMETERS

TRANSISTOR	PROCESS PARAMETERS
nMOS	LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6 XJ=0.15U RS=417 RSH=2.73 LD=0.04U VMAX=130E3 NSUB=1.17E17 PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905 GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 AF=1 WD=0.11U DELTA=0.42 NFS=1.2E11
pMOS	LEVEL=3 UO=100 TOX=1.0E-8 TPG=1 VTO=0.58 JS=0.38E-6 XJ=0.10U RS=886 RSH=1.81 LD=0.03U VMAX=113E3 NSUB=2.08E17 PB=0.911 ETA=0.00 THETA=0.120 PHI=0.905 GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 AF=1 WD=0.14U DELTA=0.81 NFS=0.52E11

[1] Lossy Current Integrator: For the circuit shown in Figure 2 the ac analysis were carried out with the value of dc bias current I_B = 15µA, C = 1pF, (W/L) ratio = 1µm/1µm and supply voltage V_{DD} = 2.5V. The value of cut-off frequency was found to be f_O = 3.5364MHz which was very well in agreement with the calculated theoretical value of f_O = 3.5MHz. SPICE simulation results are shown in Figure-7. Figure-8 shows the change in the value of cut-off frequency with change in the value of capacitor. Figure-9 shows the change in the value of gain with change in the value of bias current.

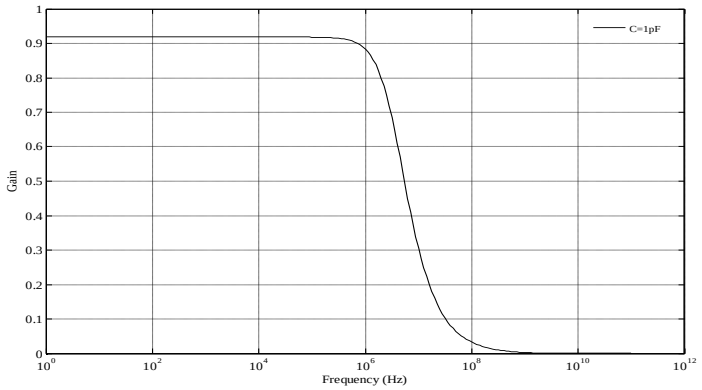

Fig. 7: First order Low Pass Response of Lossy Current Integrator

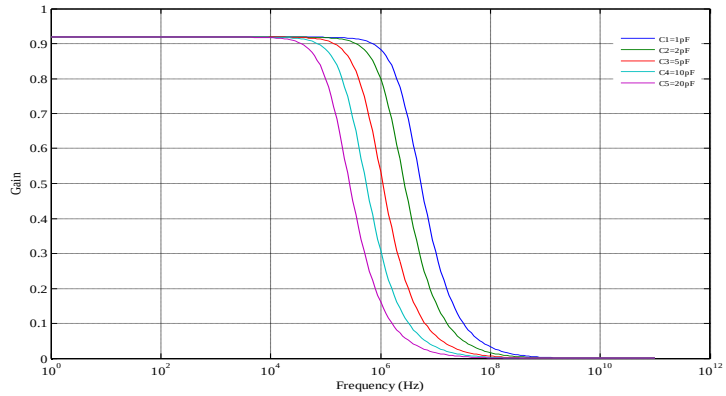

Fig. 8: Variation in cut-off frequency of Lossy Current Integrator with capacitor

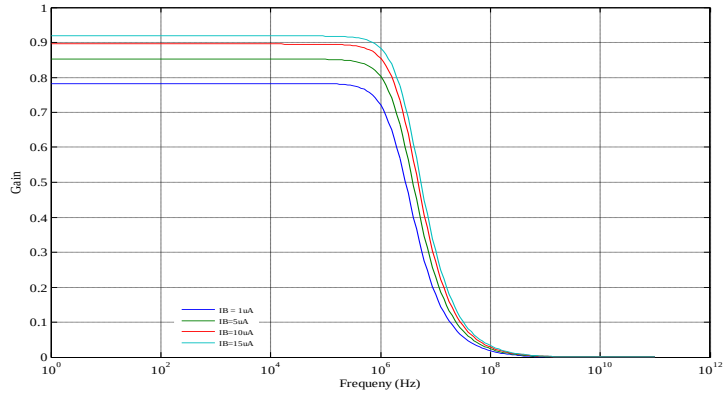

Fig. 9: Variation in gain of Lossy Current Integrator with bias current

[2] Simplified Lossy Current Integrator: For the circuit shown in Figure 4 the ac analysis were carried out with the value of dc bias current I_B = 40µA, C = 1pF, (W/L) ratio = 1µm/1µm and supply voltage V_{DD} = 2.5V. The value of cut-off frequency was found to be f_O = 4.445MHz which was very well in agreement with the calculated theoretical value of f_O = 4.5MHz. SPICE simulation results are shown in Figure-10. Figure-11 shows the output of the circuit for a square input of amplitude 5µA peak value and a period of 10µs.

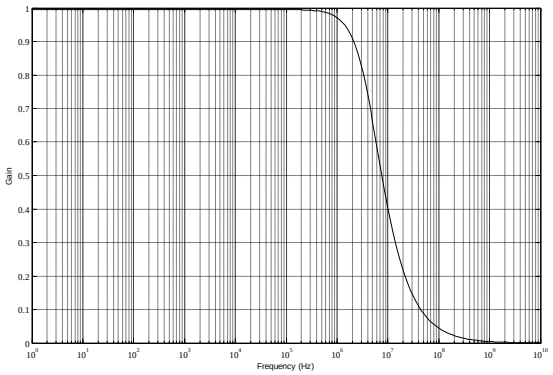

Fig. 10: First order Low Pass Response of Simplified Lossy Current Integrator

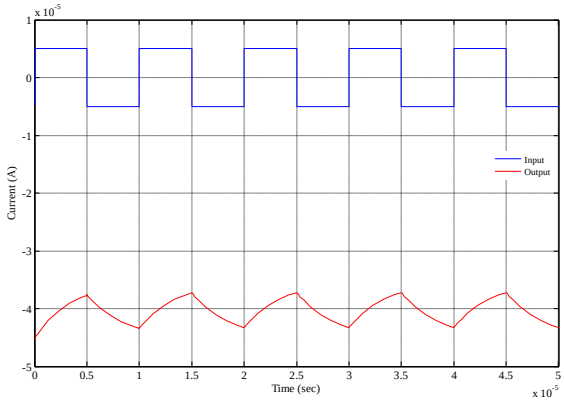

Fig. 11 Response of Simplified Lossy Current Integrator for Square input

[3] Lossless Current Integrator Type-I (Ideal Current Integrator): For the circuit shown in Figure 5 the ac analysis were carried out with the value of dc bias current I_B = 1µA, C = 1pF, (W/L) ratio of pMOS transistor = 1µm/1µm, (W/L) ratio of nMOS transistor = 1.5µm/10µm and supply voltage V_{DD} = 2.5V. The value of cut-off frequency was found to be f_O = 1.9083MHz which was very well in agreement with the calculated theoretical value of f_O = 2.0MHz. SPICE simulation results are shown in Figure-12. Figure-13 shows the change in the value of cut-off frequency with change in the value of capacitor. Figure-14 shows the change in the value of gain with change in the value of bias current while Figure 15 shows the integrator response for a square input of amplitude 2.5µA peak value and period of 20µs.

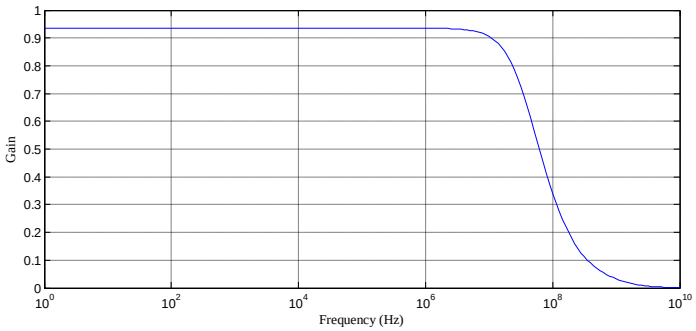

Fig. 12: First Order Low Pass Response of Lossless Current Integrator (Type-I)

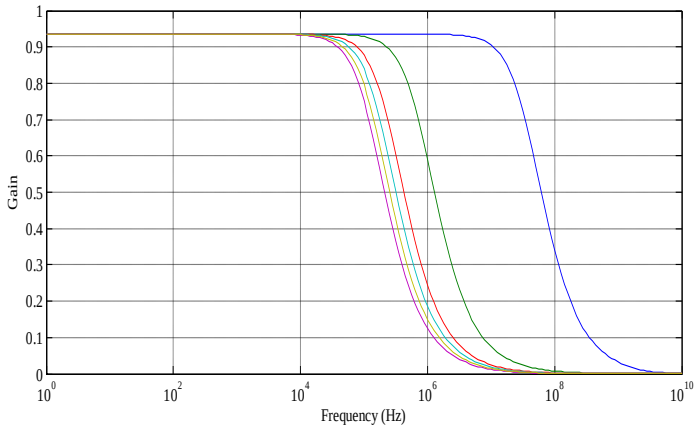

Fig. 13: First Order Low Pass Response of Lossless Current Integrator (Type-I) for different value of capacitors

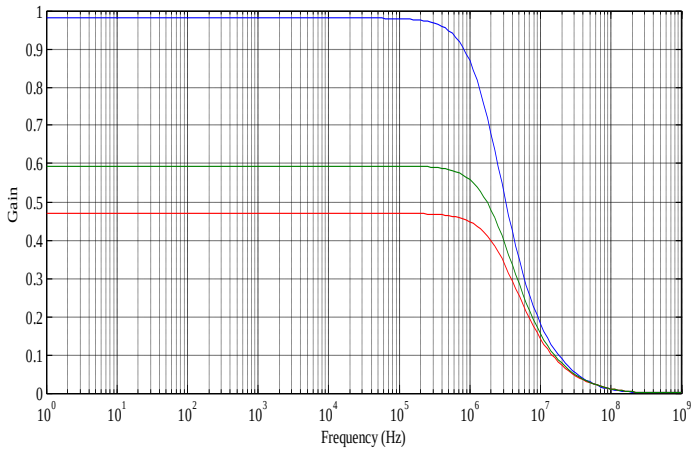

Fig. 14: First Order Low Pass Response of Lossless Current Integrator (Type-I) for various input bias currents

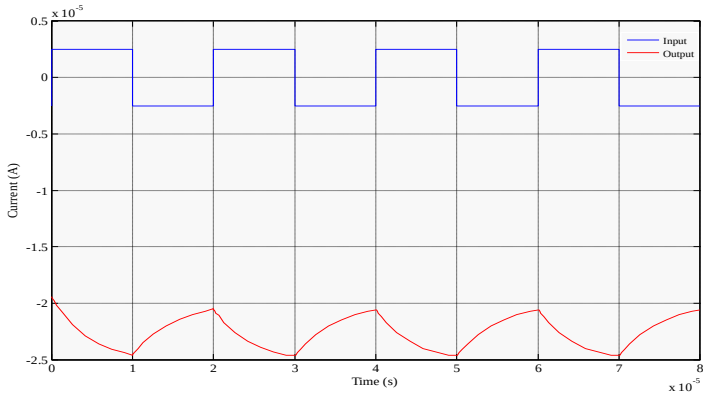

Fig. 15: Response of Lossless Current Integrator (Type-I) for Square input

[3] Lossless Current Integrator Type-II (Ideal Current Integrator): For the circuit shown in Figure 6 various analysis were carried out with the value of dc bias current I_B = 1µA, C = 0.1nF, (W/L) ratio of pMOS transistor = 1.0µm/1.0µm, (W/L) ratio of nMOS transistor = 1.0µm/1.0µm and supply voltage V_{DD} = 2.5V. SPICE simulation results shown in Figure-16 represents the response of lossless integrator circuit for a sinusoidal input of peak amplitude 10µA and a frequency of 100KHz. Figure-17 represents the response of lossless integrator circuit for a square input of peak amplitude 5µA and a period of 20µs.

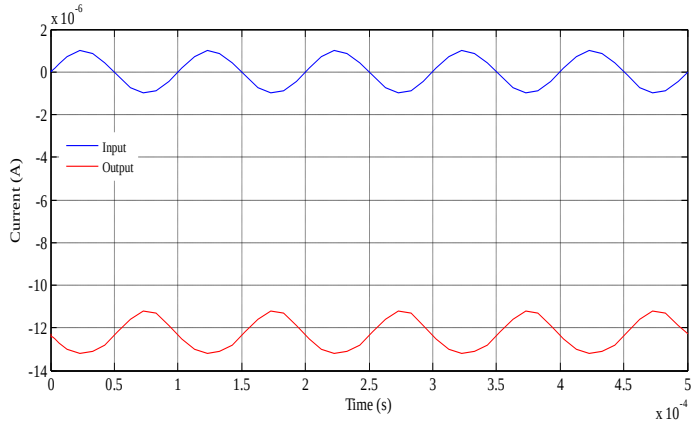

Fig. 16: Response of Lossless Current Integrator (Type-II) for Sinusoidal input

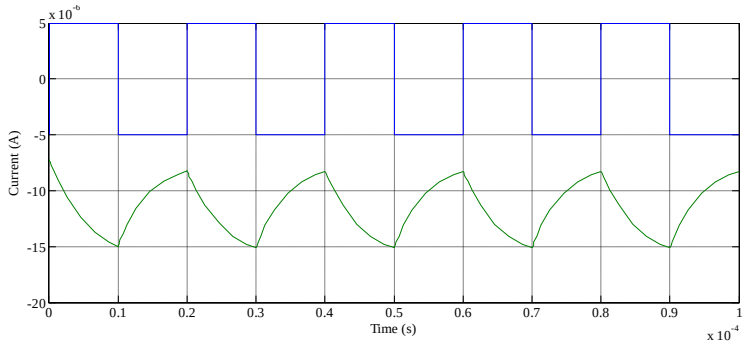

Fig. 17: Response of Lossless Current Integrator (Type-II) for Square input

IV. CONCLUSIONS

In the given paper current-mode building blocks such as current adders and current integrators (lossy and lossless) have been presented which can be used to form active filters. These active filters are quite suitable for the realization in high frequencies of more than 10MHz. and these filters can operate at a voltage as low as 1.5V or less. The frequency of these filters can be easily and widely controlled by a single DC bias current and this provides good tunability. All the circuits were tested using SPICE and the verified results confirms the theoretical values.

REFERENCES

[1]. J. C. Ahn, and N. Fujii, "Current-mode continuous-time filters using complementary current mirror pairs", IEICE Trans Fundamentals, vol. E79-A, no.2, pp.168-175, 1996.

[2]. R. Angulo, M. Robinson, and E. S. Sinencio, "Current-mode continuous-time filters: two design approaches", IEEE Tran. On Circuits and Systems, vol. 39, no. 5, pp. 337-341, 1992.

[3]. R. W. J. Barker, "Accuracy of current mirrors", IEE Colloquium on Current-mode Analogue Circuits, London, vol.25, paper 2, 1989.

[4]. B. Gilbert "Wideband negative-current mirror", Electron Lett., vol.11, pp. 126-127, 1975.

[5]. J. B. Hughes, N. C. Bird, and I. C. Macbeth, "Switched-current: a new technique for analogue sampled-data signal processing", IEEE Proc. ISCAS'89, pp. 1584-1587, 1989.

[6]. J. B. Hughes, I. C. Macbeth, and D. M. Pattullo, "Second generation switched-current signal processing", IEEE Intl. Symposium on Circuits and Systems, 1990.

[7]. D. G. Haig, and J. T. Taylor, "Continuous-time and switched capacitor monolithic filters based on current and charge simulation", IEEE International Symposium on Circuits and Systems, Portland, USA, vol.3, pp. 1580-1583, 1989.

[8]. S. S. Lee, R. H. Zele, D. J. Allstot, and G. Liang, "A continuous-time current-mode integrator", IEEE Trans. On Circuits and Systems, vol.39, pp. 1236-1238, 1991.

[9]. S. S. Lee, R. H. Zele, D. J. Allstot, and G. Liang, "CMOS continuous-time current-mode filters for high frequency applications", IEEE J. Solid State Circuits, vol.28, no.3, pp. 323-329, 1993.

[10]. M. K. N. Rao, and J. W. Haslett, "A modified current mirror with level shifting capability and low input impedance", IEEE J., vol. 14, pp. 762-764, 1979.

[11]. C. Toumazou, F. J. Lidgey, and D. G. Haigh, "Analogue IC Design: The current-mode approach", Peter Peregrinus Ltd., 1990.

[12]. Y. P. Tsividis, "Integrated continuous-time filter design-an overview", IEEE Journal of Solid-State Circuits, vol.29, issue 3, pp. 166-176, 1994.

[13]. T. Voo, and C. Toumazou, "High-speed current mirror resistive compensation technique", Electronic Letters, vol.31, no.4, pp. 248-249, 1995.

[14]. T. Voo, and C. Toumazou, C. (1996) "Efficient tunable continuous-time integrated current-mode filter designs", IEEE International Symposium on Circuits and Systems, ISCAS '96., Vol. 1, pp. 93 – 96, 1996.

[15]. Z. Wang, and W. Guggenbuhl, "Adjustable bidirectional MOS current mirror/amplifier", Electron Lett., vol.25, pp. 673-675, 1989.

[16]. B. Wilson, "Current mirrors, amplifiers and dumpers", Wireless world, vol.87, pp. 47-50, 1981.

[17]. B. Wilson, "Design current-output amplifiers using current-mirror circuits", Electron. Des. News, vol.27, pp. 121-124, 1982.

[18]. A. M. Ismail, and A. M. Soliman, "Novel CMOS Current Feedback Op-Amp Realization Suitable for High Frequency Applications", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and applications, vol. 47, No. 6, pp. 918-921, 2000.

[19]. M. Desai, P. Aronhime, and K. Zurada, "Current-mode network transformation", IEEE Proc. ISCAS'94, pp. 599-602, 1994.

[20]. R. J. Angulo, and E. S. Sinencio, "Active compensation of operational transconductance amplifier using partial positive feedback", IEEE J. of Solid-state Circuits, vol.25, pp. 1024-1028, 1990.