International Journal of Engineering Research and Development (IJERD) ISSN: 2278-067X
Recent trends in Electrical and Electronics & Communication Engineering (Page 63-68)
(RTEECE 08th – 09th April 2016)

Design and Analysis of Cascaded H-Bridge Five Level Inverter

Parth Joshi[1], Hasmukh Katariya[2], Asst. Prof. Grishma Shah[3]
[1 2] *B.E. Student Of Electrical Department, Institute Of Technology And Management-Vadodara, Gujarat*
[3]*Asst. Professor Of Electrical Department, Institute Of Technology And Management –Vadodara, Gujarat*

Abstract*: - The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as Inverter. Multilevel Inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. Multilevel Inverter has advantage like minimum harmonic distortion. Multi-level inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the stair–case voltage waveform which has reduced harmonic content. This paper aims to extend the knowledge about the performance of Five Level Cascaded H-Bridge MLI topology using SPWM for fixed DC Source. The output voltage is the sum of the voltage that is generated by each bridge. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. Results of experiments proved efficiency of 95%.The performance of the proposed SPWM strategy in terms of output voltage and THD has studied successfully and shown using MATLAB/Simulink.*

Keywords*:-Multi level Inverter (MLI), Sinusoidal Pulse Width Modulation (SPWM), Metal oxide semiconductor field effect transistor (MOSFET), Cascaded H-Bridge (CHB)*

I. INTRODUCTION

Using power electronics device an inverter is basically a device that converts DC source of energy form into that of AC source of energy form. The purpose of DC-AC inverter is to take DC source supply of power from a battery source and converts it to AC Source of energy supply. The household inverter receives DC supply from a 24V battery and then the inverter converts it to 240V AC with a desirable frequency of 50Hz. The control strategies employed in the DC-AC (i.e. the inverter) is same as that in the DC-DC Converters (i.e. Chopper). We can use both Current mode control and Voltage mode control in the practical applications. The Inverter produces an Ac output waveform from a DC Waveform.

The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. Several combinational designs have also emerged some involving cascading the fundamental topologies.

These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years. Moreover, abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In addition, many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Universal Power Conditioner and traction drive systems

II. CASCADED H-BRIDGE INVERTER

For small size inverters two level inverters are useful. But it is uneconomical and switching loss are higher when same two level inverter can be used for medium and high capacity industrial inverter. While we are using less switches for high power inverter then voltage stress and current from the switch is very high so switching loss is higher. So for high power application we are using multilevel inverter topology, In Multilevel inverter more than one source required in cascaded H-bridge inverter (source equal to number of bridge) .

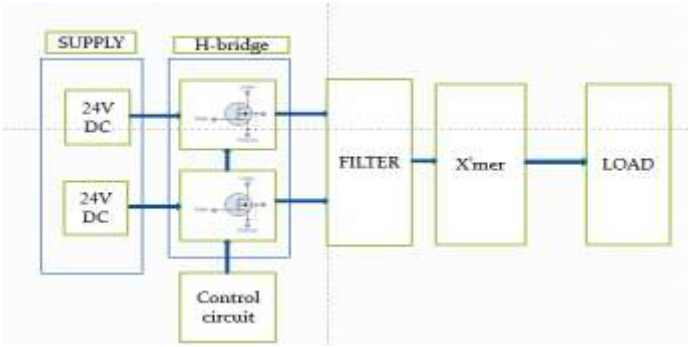

Fig 1: Block diagram of 5 level H-bridge Inverter

The main feature of multilevel inverter is as below:

- Harmonic content decreases as the number of levels increases thus reducing the filtering requirements.
- Without an increase in the rating of an individual device, the output Voltage and power can be increased.
- The switching devices do not encounter any voltage sharing problems.
- They have higher efficiency because the devices can be switched at Low frequency.

III. CASCADED 5 LEVEL H BRIDGE MULTILEVEL INVERTER

A hybrid H-bridge inverter consists of a series of H-bridge inverter units. The general function of this Multi-level inverter is to synthesize a desired voltage form several DC sources (SDCSs). Each SDCS is connected to an H-bridge inverter. The AC terminal voltages of different level inverters are connected in series. Unlike diode clamp or flying capacitors inverters the hybrid H-bridge inverter does not require any voltage clamping diodes or voltage-balancing capacitors.

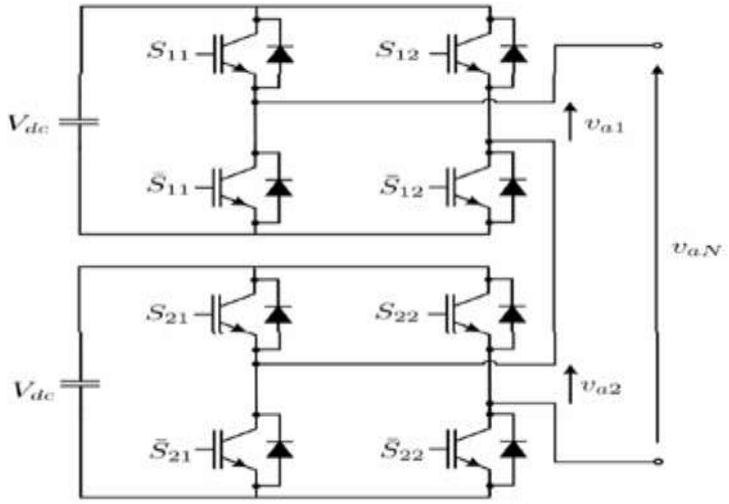

Fig: 2 : circuit of 5 level H bridge inverter

Figure shows the synthesized phase voltage waveform of five-level hybrid H-bridge inverter with two bride connected in series. The phase output voltage is synthesized by the sum of the two inverter outputs, Van = Va1+Va2. Each inverter circuit can generate three different outputs, +Vdc , 0 , -Vdc . Multilevel inverter consist of 8 switch.(four switch for each bridge). To obtain +Vdc, switches S11 and -S12 are turned on, whereas –Vdc can be obtained by turning on switches S_{12} and $–S_{11}$. By turning on S11 and S12 or $–S_{11}$ and -S12, the output voltage is 0. Similarly S_{21} and $-S_{22}$ for +Vdc, switches S_{22} and -S21 are turned on for –Vdc. The ac outputs of each of the different full-bridge inverter levels are connected in series. And the output is sum of that two inverter. the synthesized voltage waveform is the sum of the inverter outputs. As given below

No of switches	Voltage level
S_{11} , $-S_{12}$, S_{21} , $-S_{22}$	+2Vdc
S_{11} , $-S_{12}$, S_{21} , S_{22}	+Vdc
S_{11} , S_{12} , S_{21} , S_{22}	0

$-S_{11}$, S_{12} , S_{21} , $-S_{22}$	-Vdc
$-S_{11}$, S_{12} , $-S_{21}$, S_{22}	-2Vdc

IV. SIMULATION RESULTS

A) Simulation of Cascaded H bridge Inverter

Fig. shows the simulation of cascaded H bride 5 level multilevel inverter

Sr. no.	Component	block	Parameters
1	Input voltage	2 separate DC voltage source	Vdc = 24V per source
2	Power switch	MOSFET	default
3	Gate circuit	SPWM type	With 1 sine and 4 triangular wave For S_{11} -S_{11} S_{12} -S_{12}
4	Not gate	Not gate(4)	For gate pulse of S_{21} -S_{21} S_{22} -S_{22}
5	Output	(2)Scope	default

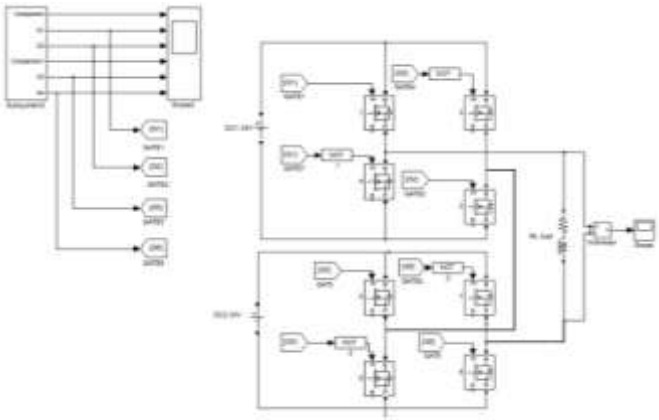

Fig 3 : Simulation of 5 level H-bridge inverter

B) Output wave forms

Scale : X axis : Time in sec.
Y axis : Voltage in volt.

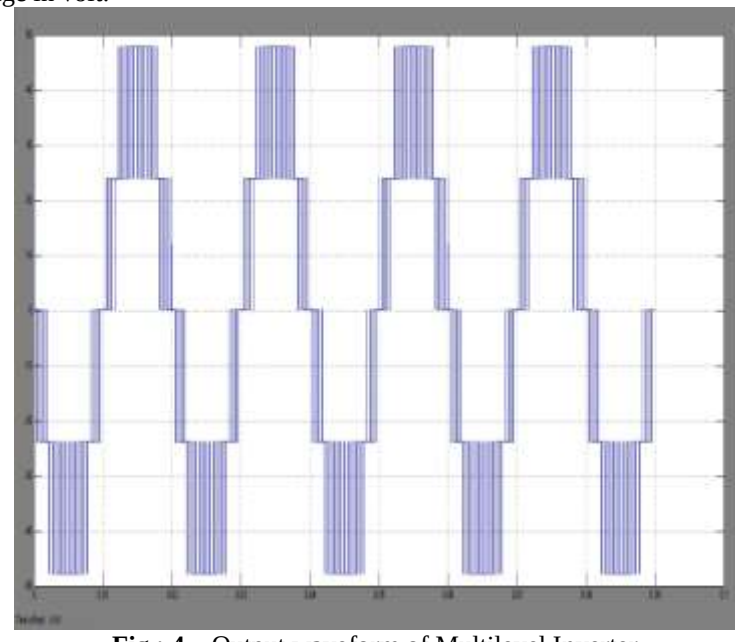

Fig : 4 – Output waveform of Multilevel Inverter

C) Gate Circuit

Sine wave –Magnitude 1.8 V
Triangular wave –Frequency 1000 Hz
Modulation Index- 0.9
2 wave with 0 degree
2 wave with 180 out of phase
Comparison of triangular and sine

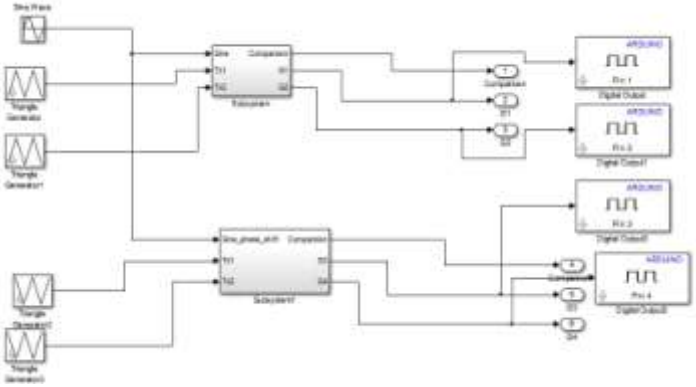

Fig: 5 – gate circuit of Multilevel inverter

D)Output Waveform of Gate Circuit

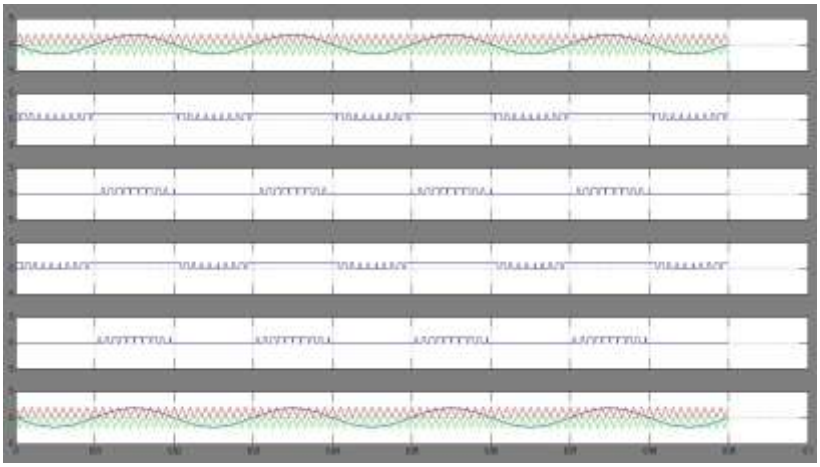

Fig 6 : Output Comparition of Gate Pulse

E) Arduino output waveforms for switches

- Gate pulse for switch S_{11} and $-S_{11}$
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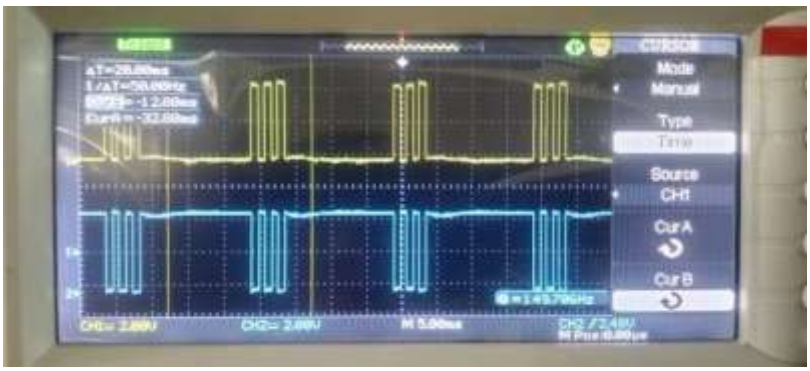

Fig 7: output in DSO of switch S_{11} and $-S_{11}$

- Gate pulse for switch S_{12} and $-S_{12}$

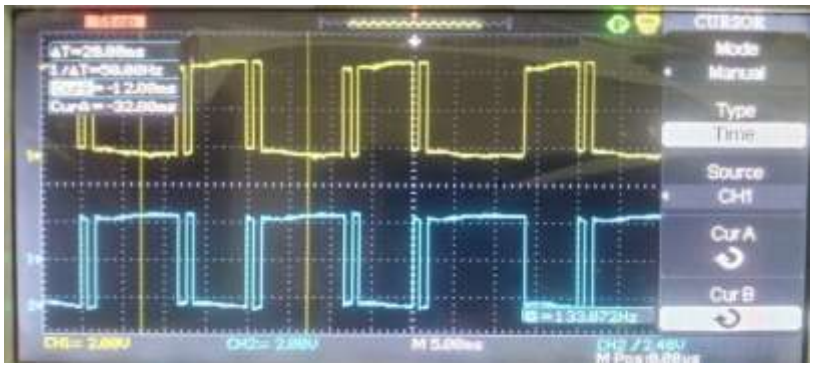

Fig 8: output in DSO of switch S_{12} and $-S_{12}$

- Gate pulse for switch S_{21} and $-S_{21}$
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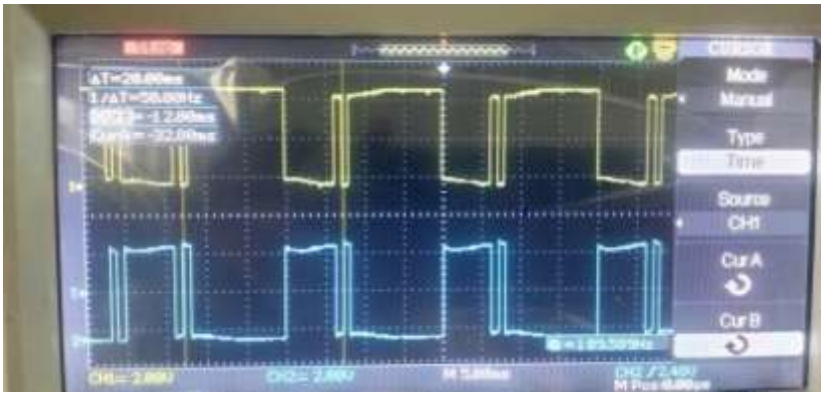

Fig 9 : Output in DSO switch S_{21} and $-S_{21}$

- Gate pulse for switch S_{22} and $-S_{22}$
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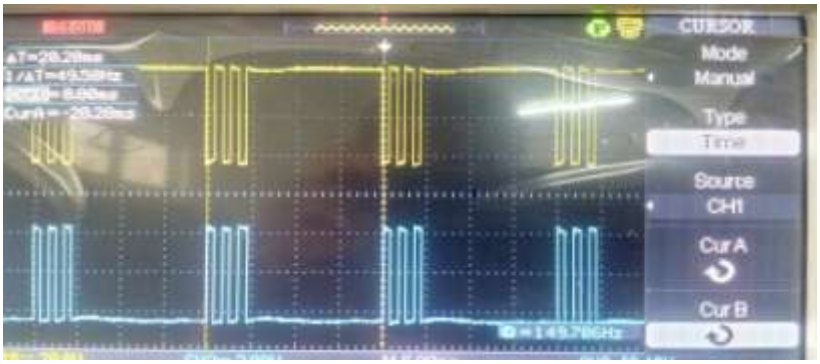

Fig 10 : output in DSO of switch S_{22} and $-S_{22}$

F) THD analysis

In the inverter total harmonics distortion (THD) is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave. THD calculations can be obtained from the SIMULINK. The switching pattern that is used in this project for all of the multilevel inverters is SPWM technique. In this method the switching angles for switches should be calculated in such a way that the dominant harmonics are eliminated (minimized). For a 5-level inverter the 5th harmonic will be eliminated.

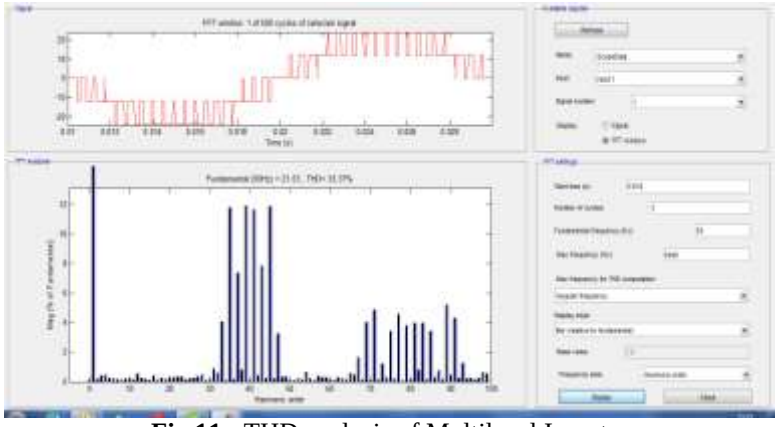

Fig 11 : THD analysis of Multilevel Inverter

V. CONCLUSION

It has been observed from the simulation results which are more than the conventional DC to AC 2 level inverter. The two-level inverter has the lowest cost and weight in comparison with the other topologies. With compared to other multilevel topology this method is more easy and more reliable. Components required for these topology is also less compared to other topology. The design of the 5-level multilevel inverters seems to be better than the 9-level multilevel inverters. By increasing the number of levels, the cost and weight of the multilevel inverter will be increased. So this topology is well suited for industrial drives.

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