International Journal of Engineering Research and Development
e-ISSN: 2278-067X, p-ISSN: 2278-800X, www.ijerd.com
Volume 10, Issue 2 (February 2014), PP.106-111

Common-Mode Leakage Current Eliminated Photovoltaic Grid-Connected Power System for Domestic Distribution

Ajith Ashokan[1],Bos Mathew Jos[2], Benny Cherian[3]
[1]*MTech student, power electronics, Mar Athanasius College of engineering, Kothamangalam*
[2,3]*Professor, Mar Athanasius College of engineering, Kothamangalam*

Abstract:- Improved single-phase inverter topology is used to avoid the common-mode leakage current in the transformerless PV grid-connected system. The condition of eliminating common-mode leakage current in both the unipolar sinusoidal pulse width modulation (SPWM) and the double frequency SPWM control method can be applied to implement AC output in the presented inverter. By decoupling of two additional switches connected to the dc side the efficiency and convenient thermal design are improved. Besides, the higher frequency and lower current ripples are obtained by adopting the double-frequency SPWM, and thus the total harmonic distortion of the grid-connected current are reduced to 7%. It is used for low ac power application. Working of the proposed circuit and verification by simulation results are discussed in this paper. Simulation is done in MATLAB.

Keywords:- Common-mode leakage current, photovoltaic (PV) system, sinusoidal pulse width modulation (SPWM) strategy, transformer less inverter, buck.

I. INTRODUCTION

The need for a cleaner environment and the continuous increase in energy needs makes decentralized renewable energy production more and more important. This continuously-increasing energy consumption overloads the distribution grids as well as the power stations, therefore having a negative impact on power availability, security and quality. One of the solutions for overcoming this is the Distributed Generation (DG) system. DG systems using renewable energy sources like solar PV system is still much more expensive than traditional ones, due to the high manufacturing costs of PV panels, but the energy that drives them -the light from the sun- is free, available almost everywhere and will still be present for millions of years, advantages of PV technology is that it has no moving parts. Therefore, the hardware is very robust; it has a long lifetime and low maintenance requirements [1]. A common mode leakage current flows through parasitic capacitor between the PV arrays. To avoid the common-mode leakage current, a high voltage DC is converted by buck DC/DC and connected full bridge improved inverter with unipolar SPWM [2]-[6]. A high voltage input approximately, 400V for $220V_{ac}$ application. A power electronic converter uses semiconductor devices to transform power from one form to another form. A buck converter is a specific type of dc-dc power electronic converter whose goal is to efficiently step down DC voltage to a lower level with minimal ripple. Typically the buck converter employs feedback to regulate the output voltage in the presence of load changes. This improvement in performance over voltage dividers and regulators comes at the cost of additional components and complexity. In the remainder of this handout, we will examine the characteristics of the buck chopper and derive relationships and tools necessary to properly specify the components required to implement a desired design.

II. CONDITION OF ELIMINATING COMMON-MODE LEAKAGE CURRENT

Without an isolated transformer in the PV grid-connected power systems, there is a galvanic connection between the grid and the PV array, which may form a common-mode resonant circuit and induce the common-mode leakage current. The common-mode voltage can be defined as the average of the sum of voltages between the outputs and the common reference. In this case, the common reference is taken to be the negative terminal of the PV

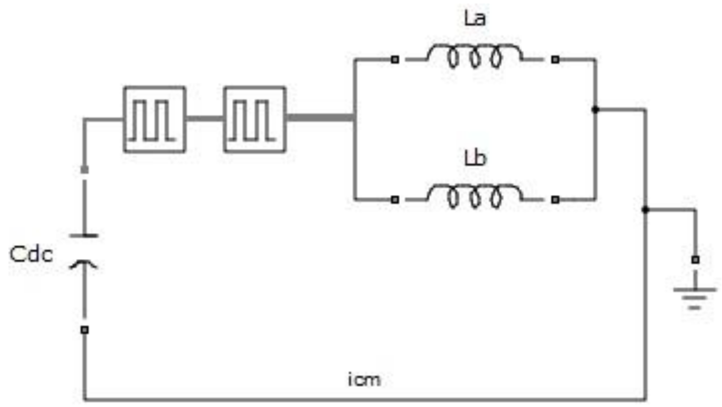


Fig. 1: The simplified equivalent model of the common-mode resonant circuit

(1) $$u_{cm} = \frac{u_{AN} + u_{BN}}{2}$$

The differential-mode voltage is defined as the difference between the two voltages.

(2) $$u_{dm} = u_{AB} = u_{AN} - u_{BN}$$

The simplified equivalent model of the common-mode resonant circuit has been derived in as shown in Fig.1, where C_{dc} is the parasitic capacitor, L_A and L_B are the filter inductors, I_{cm} is the common-mode leakage current. And, an equivalent common-mode voltage U_{ecm} is defined by,

(3) $$u_{ecm} = u_{cm} + \frac{u_{dm}}{2}\frac{L_B - L_A}{L_A + L_B}$$

It is clear that the common-mode leakage current I_{cm} is excited by the defined equivalent common-mode voltage u_{ecm} . Therefore, the condition of eliminating common-mode leakage current is drawn that the equivalent common-mode voltage u_{ecm} must be kept a constant as follows,

$$= \frac{u_{AN} + u_{BN}}{2} + \frac{u_{AN} - u_{BN}}{2}\frac{L_B - L_A}{L_A + L_B} = \text{Constant} \quad (4)$$

In the half-bridge inverter family, one of the filter inductors L_A and L_B is commonly zero. Therefore, the condition of eliminating common-mode leakage current is accordingly met that,

$$u_{ecm} = \frac{u_{AN} + u_{BN}}{2} + \frac{u_{AN} - u_{BN}}{2} = u_{AN} = \quad \text{constant } (L_A = 0) \quad (5)$$

$$u_{ecm} = \frac{u_{AN} + u_{BN}}{2} - \frac{u_{AN} - u_{BN}}{2} = u_{BN} = \quad \text{constant } (L_B = 0) \quad (6)$$

Similarly, in the full-bridge inverter family, the filter inductors L_A and L_B are commonly selected with the same value. As a result, the condition of eliminating common-mode leakage current is met that [1],

$$u_{cem} = u_{cm} = \frac{u_{AN} + u_{BN}}{2} = \quad \text{constant } (L_A = L_B) \quad (7)$$

III. IMPROVED INVERTER TOPOLOGY AND OPERATION MODES

Fig.2. shows the improved grid-connected inverter topology, which can meet the condition of eliminating common-mode leakage current. In this topology, two additional switches S_5 and S_6 are symmetrically added to the conventional full-bridge inverter, and the unipolar SPWM and double-frequency SPWM strategies with three-level output can be achieved.

A. UNIPOLAR SPWM STRATEGY

Like the full-bridge inverter with unipolar SPWM, the improved inverter has one phase leg including S_1 and S_2 operating at the grid frequency, and another phase leg including S_3 and S_4 commutating at the switching frequency. Two additional switches S_5 and S_6 commutate alternately at the grid frequency and the switching frequency to achieve the dc-decoupling states. Accordingly, four operation modes that generate the voltage states of $+U_{dc}$, 0, $-U_{dc}$.

MODE 1: when S_4 and S_5 are ON, $U_{AB} = +U_{dc}$ and the inductor current increases through the switches S_5, S_1 , S_4 , and S_6 . The common-mode voltage is

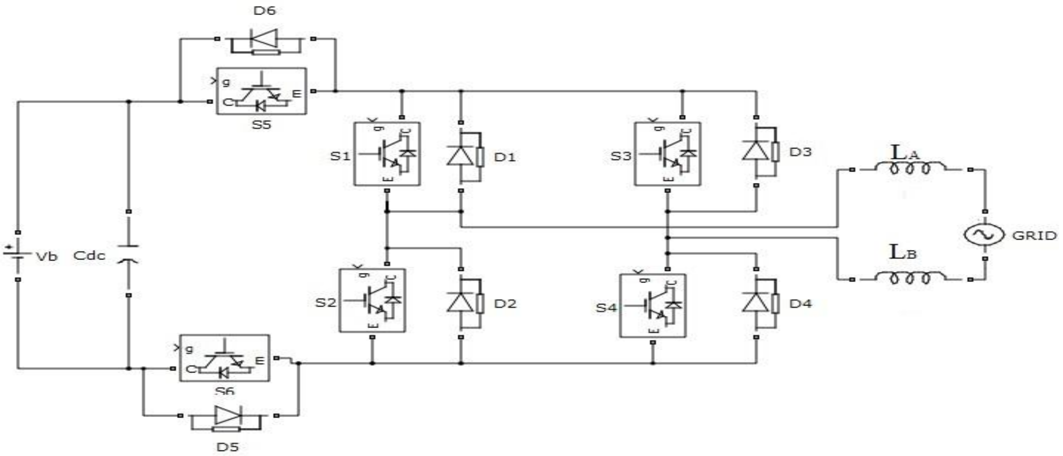


Fig. 2: Improved inverter topology

$$u_{cm} = \frac{1}{2}\left(u_{AN} + u_{BN}\right) = \frac{1}{2}\left(u_{dc} + 0\right) = \frac{u_{dc}}{2} \tag{8}$$

MODE 2: when S_4 and S_5 are turned OFF, the voltage U_{AN} falls and U_{BN} rises until their values are equal, and the antiparallel diode of S_3 conducts. Therefore, U_{AB} = 0V and the inductor current decreases through the switch S_1 and the antiparallel diode of S_3 . The common-mode voltage changes into

$$u_{cm} = \frac{1}{2}\left(u_{AN} + u_{BN}\right) = \frac{1}{2}\left(\frac{u_{dc}}{2} + \frac{u_{dc}}{2}\right) = \frac{u_{dc}}{2} \tag{9}$$

MODE 3: when S_3 and S_6 are ON, $U_{AB} = -U_{dc}$ and the inductor current increases reversely through the switches S_5 , S_3 , S_2 , and S_6 . The common-mode voltage becomes

$$u_{cm} = \frac{1}{2}\left(u_{AN} + u_{BN}\right) = \frac{1}{2}\left(0 + u_{dc}\right) = \frac{u_{dc}}{2} \tag{10}$$

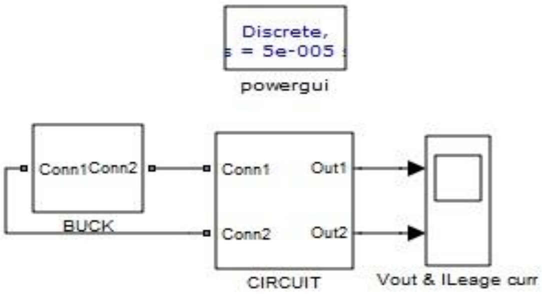
MODE 4: when S_3 and S_6 are turned OFF, the voltage U_{AN} rises and U_{BN} falls until their values are equal, and the antiparallel diode of S_4 conducts. Similar as to Mode 2, U_{AB} = 0V and the inductor current decreases through the switch S_2 and the antiparallel diode of S_4 . The common-mode voltage u_{cm} also keeps $U_{dc}/2$.

$$u_{cm} = \frac{1}{2}\left(u_{AN} + u_{BN}\right) = \frac{1}{2}\left(\frac{u_{dc}}{2} + \frac{u_{dc}}{2}\right) = \frac{u_{dc}}{2} \tag{11}$$

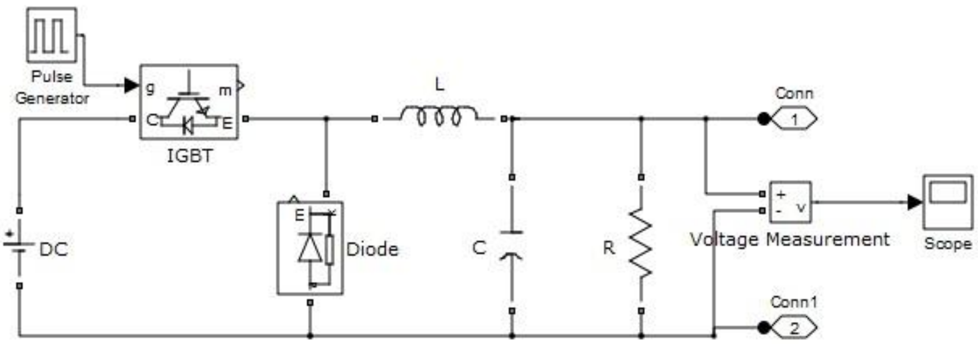
In ideal wave form, in the positive half cycle, S_1 and S_6 are always ON. S_4 and S_5 commutate at the switching frequency with the same commutation orders. S_2 and S_3, respectively, commutate complementarily to S_1 and S_4. Accordingly, Mode 1 and Mode 2 continuously rotate to generate $+U_{dc}$ and zero states and modulate the output voltage. Likewise, in the negative half cycle, Mode 3 and Mode 4 continuously rotate to generate $-U_{dc}$ and zero states as a result of the symmetrical modulation [1].

IV. SIMULINK MODEL

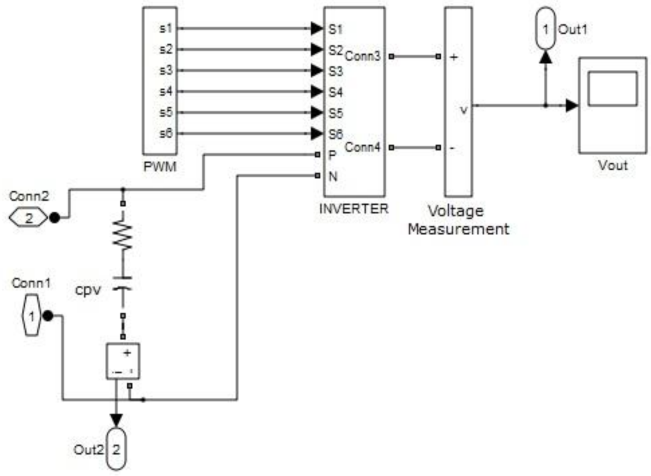
In fig 3(a) shows the main circuit of system. This is a 2subsystem and one output scope, block, 1st one is BUCK and another one is inverting circuit, and output signal is connected into scope. The output shows voltage across AB point and current through parasitic capacitors. Fig 3(b) represent BUCK converter, its convert 400V to 200V, DC-DC converter. LC is used for filter. Fig 3(c) shows the inverting circuit, it gives input from output of the buck convert. Parasitic capacitor connected across the input voltage and checks the current through it. This is common mode leakage current. This current is almost equal to zero. Fig 3(d) shows the internal circuit of inverter switches S_1-S_6 is connected. This is converting DC-AC, from 200V dc to 200 ac. For working IGBT, gate signal is applied by SPWM.



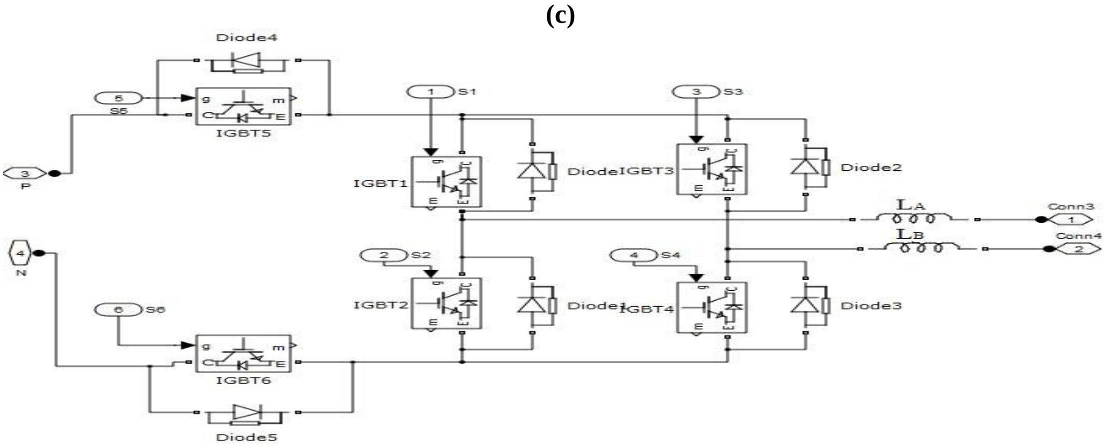
(a)



(b)



(c)



(d)

Fig. 3: Simulink of (a) main model (b) buck circuit (c) main circuit (d) inverter circuit

V. SIMULATION RESULTS AND ANALYSIS

For simulation, following components are used: L_f=4mH, L_{f1}=4mH, C_{dc} =75nF V_{dc}=400V, grid frequency, f_g =50 Hz; switch frequency, f_s = 20 kHz By using these components the input voltage is converted into ac source. Here DC is stepdowned by using buck and converter. In buck converter, an LC filter with L= 47µH, C=47µF. A high voltage DC is convert into low voltage DC V_b=200VC. This voltage is converted into grid voltage, *Ug* =200 V ac;

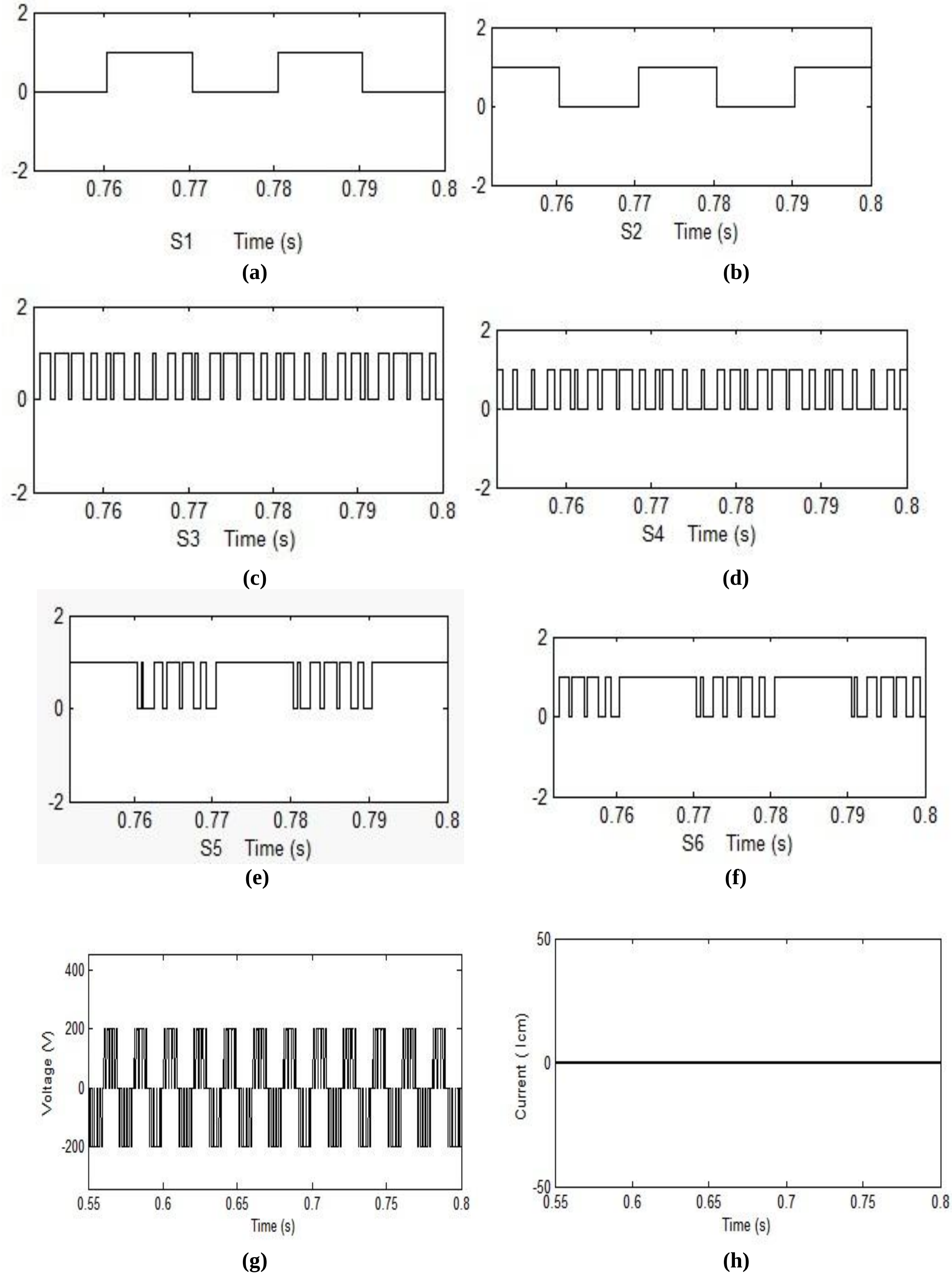


Fig. 4: Simulated waveforms of (a) switch S_1, (b) switch S_2 (c) switch S_3 (d) switch S_4 (e) switch S_5, (f) switch S_6 (g) V_{out}, (h) I_{cm}.

VI. CONCLUSION

This paper presents an improved grid-connected inverter topology for transformerless PV systems. The unipolar SPWM control method is implemented, which can guarantee not to generate the common-mode leakage current because the condition of eliminating common-mode leakage current is met completely. Moreover, the switching voltages of all commutating switches are half of the input dc voltage and the switching losses are reduced greatly. The high efficiency and convenient thermal design are achieved by the decoupling of two additional switches *S*5 and *S*6. It is used low ac power application. Working of the proposed circuit and verification by simulation results are discussed in this paper. Simulation is done in MATLAB.

REFERENCES

[1]. Bo Yang, Wuhua Li, Yunjie Gu, Wenfeng Cui, and Xiangning “Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System” IEEE Transactions On Power Electronics, Vol. 27, No. 2, February 2012

[2]. S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A review of single-phase grid-connected inverters for photovoltaic modules,” IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005

[3]. Q. Li and P.Wolfs, “A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations,” *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[4]. H. Xiao and S. Xie, “Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter,” *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov. 2010

[5]. T. Kerekes, R. Teodorescu, and M. Liserre, “Common mode voltage incase of transformerless PV inverters connected to the grid,” in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun./Jul. 2008, pp. 2390–2395

[6]. R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, “Transformerless inverter for single-phase photovoltaic systems,” *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007