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Efficient Pc Controlled By Hand Movement Using Mems Sensor Mouse

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Abstract:- Ahybrid two-dimensional position sensing system is designed for mouse applications. The system measures the acceleration of hand- movements which are converted into two-dimensional location coordinates. The system consists of four major components: 1) MEMS accelerometers, 2) CMOS analog read-out circuitry, 3) an acceleration magnitude extraction module, and 4) a 16-bit RISC microprocessor. Mechanical and analog circuit simulation shows that the designed padless mouse system can detect accelerations as small as 5.3 mg and operate up to 18MHz.

I. INTRODUCTION

Most commercial mouse systems are built with rolling-ball or optical technology to provide cursor positions. For example, a ball mouse system detects physical rolling movements of the ball, which are affected by a non-flat or obstructed surface. An optical mouse system avoids these environmental factors by detecting the reflec- tion of light on a reflective supplementary pad. Both technologies, however, require a special surface limiting the working space and freedom of the user's movements. Obviously, a more desirable mouse system would not be restricted by environmental factors.

In this paper, we describe a novel mouse system design which detects two-dimensional positions without any additional compo- nents such as pads. Shown in Figure 1, the system consists of four major components: 1) MEMS (Micro Electro Mechanical Systems) accelerometers, 2) CMOS analog read-out circuitry, 3) an accelera- tion magnitude extraction module, and 4) a 16-bit RISC micropro- cessor. Two MEMS accelerometer devices are employed to measure *X* and *Y*-axis acceleration of the movements from the user's hand. These acceleration values are pulse-width modulated by the CMOS analog read-out circuitry and will be converted into (*X, Y*) coordi- nates on the screen by performing integral operations using a 16-bit RISC microprocessor. In this design, we present a hybrid configura- tion system, which means each component is not based on the same substrate and thus has to be interfaced with each other by means of external connections. The MEMS device is designed in S.O.G. (Sil- icon On Glass) technology developed at the University of Michigan. The analog readout circuit is designed in a dual-poly, single-metal process, also developed at the University of Michigan and the digital microprocessor is designed in a 1.5□ □m AMI process through MOSIS using SCMOS design rules.

The rest of this paper is organized as follows. Section 2 presentstion 5 describes monolithic implementation of the mouse as future work with conclusion in Section 6.

II. SYSTEM OVERVIEW

2.1 System Requirements and Constraints

Two system requirements stand out for consideration: *speed* and *accuracy.* Generally the speed of physical reaction from a human is remarkably slow compared to the speed of a modern microprocessor and it is reported that the magnitude of an action is at most on the order of 10^{-2} seconds [1]. Since the mouse system must generate (*X, Y*) coordinate values faster than this rate, the target clock frequency was chosen to be 100 kHz, which provides 500 instructions per coor- dinate calculation. In terms of movement accuracy, the finest accel- eration from a human hand is more than 10 mg ($g=9.8m/s^2$). One of the most important figures of merit in MEMS accelerometers is sen- sitivity which is defined as the capacitance variation per acceleration change. The capacitance change due to acceleration input is detected and converted to a voltage in analog read-out circuits. Accordingly, together with the MEMS accelerometer's sensitivity, the gain and equivalent input noise of the analog read-out circuits determine the overall minimum detectable acceleration. The analog read-out cir- cuits and MEMS accelerometer are designed to detect acceleration as small as 5 mg so that our system can catch the smallest movement of the human hand.

2.2 Design Methodology

A capacitive sensing configuration, as shown in Figure 2, was chosen for the MEMS accelerometer because it gives high sensitiv- ity with low temperature drift [4]. The device dimensions optimize large

sensitivity over layout area and its functionality was verified using ANSYS.
For the analog read-out circuit design, switched capacitor circuits were chosen to simplify the interface between the analog and the digital parts. All the analog circuit designs were simulated with HSPICE and laid out using Mentor Graphics software.

A top-down approach was used to partition the design into its var- ious analog, digital, and MEMS components. Each module was ver- ified using a bottom-up approach for timing, functionality, and LVS. The majority of modules—the microprocessor datapath, analog cir- cuitry, and MEMS devices—are full custom designs while The overall system architecture and explains each module in detail. Section 3 describes the verification and testing methodology for our system. Section 4 reports the statistical data of the final design. Sec-

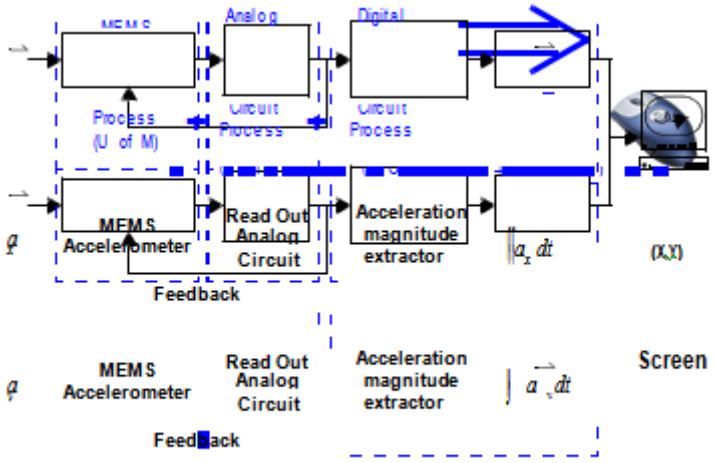


Figure1. Block diagram for the hybrid MOUSE system.

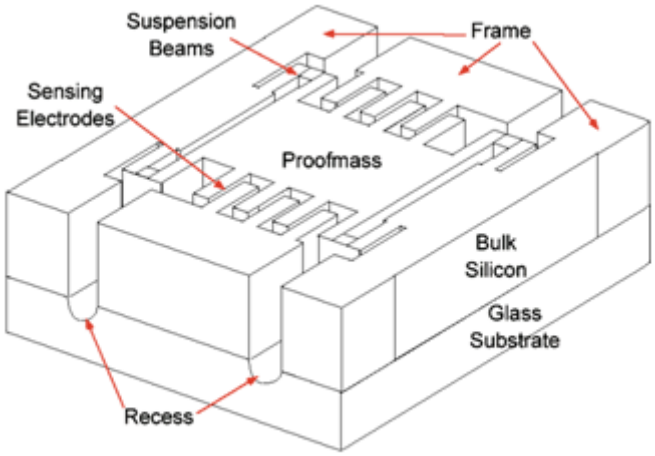


Figure 2. S.O.G MEMS accelerometer.

Microprocessor controller was designed using Verilog HDL.

2.3 Operational Overview

Figure 1 shows an operational block diagram of the mouse sys- tem. When a user moves the mouse in an arbitrary direction, the acceleration is decomposed into *X*- and *Y*-axis acceleration compo- nents by a corresponding "MEMS accelerometer". The actual accel- eration value is represented by a differential capacitance between two capacitors in the MEMS device. This capacitance value is simultaneously fed back to reset the MEMS device—so the next acceleration can be measured without any bias—and fed forward into the CMOS analog read-out circuitry where it is converted into a digital pulse-width modulated output voltage. The polarity of the pulse, either positive or negative, determines the direction of the acceleration and the width of the pulse is proportional to the magni- tude of the acceleration. An "acceleration magnitude extractor" changes the generated pulse width into the units of system clock fre- quency, which will be used by the microprocessor to calculate the exact position coordinate values on the screen.

2.4 MEMS Accelerometer

Typically, there are three different types of MEMS accelerome- ters, piezo-resistive [2], tunneling [3], and capacitive [4, 5]. The capacitive accelerometer was chosen for this system because it pro- vides high sensitivity, good DC response, low drift, low temperature sensitivity, low-power dissipation, and a simple structure [6]. S.O.G technology was chosen for the implementation, instead of some other technology, to take advantage of its robustness and simplicity of design.

Figure 2 shows the structure of a S.O.G. lateral accelerometer
[4]. A MEMS accelerometer consists of two major components: a proof mass and sensing electrodes. A proof mass and sensing elec- trodes are connected to a frame which is anchored to a glass sub- strate. Since the proof mass is suspended over a recess on a glass substrate with serpentine suspesion beams, it is free to move in response to an external acceleration. Electrodes attached to the glass substrate are stationary. When external forces are applied to the accelerometer (by the user's hand movement, for example), the proof mass moves against the forced direction due to an inertia force while the electrodes remain stationary. The movement causes capacitance variations between the comb fingers which form parallel plate capacitors, denoted as ΔC. One side of the comb fingers generates a positive variation($+\Delta C/2$), and the other side produces a negative one($-\Delta C/2$). The total capacitance change is the difference between these two values [($+\Delta C/2$)-($-\Delta C/2$)]. Therefore, the external acceler- ation is converted to the differential capacitance variation which can be expressed as:

$$\Delta C \; (F/g) = \frac{9.8 \cdot M}{k \cdot d_o} \cdot C_s \qquad (1)$$

Where M is the mass of the proof mass, C_s is the rest capacitance, d_o

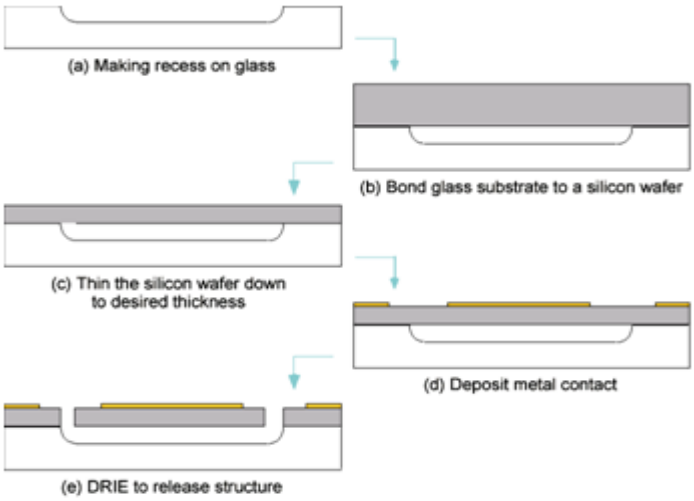


Figure 3. Fabrication process sequence

Is the sensing gap distance, and k is the spring constant of the sus- pension beams[5]. From Eqn.(1), it can be expected that a heavy accelerometer with a large number of comb fingers and compliant structure—i.e., small spring constant—provides good sensitivity, although it is difficult to fabricate such accelerometers. A single crystal silicon proof mass 2.1 mm wide, 2.4 mm long, and 100 □ m high gives 0.78 pF/g sensitivity. For the two-dimensional mouse sys- tem, two lateral accelerometers are required for sensing *X* and *Y*-axis accelerations. A schematic top view of the MEMS accelerometer in Figure 2 is shown in Figure 5.

The fabrication process has 5 steps requiring only 3 masks devel- oped at the University of Michigan. Figure 3 shows the cross section of the wafer for each fabrication step and Figure 4 shows an SEM
(Scanning Electron Microscope) picture of a MEMS accelerometer taken after fabrication.

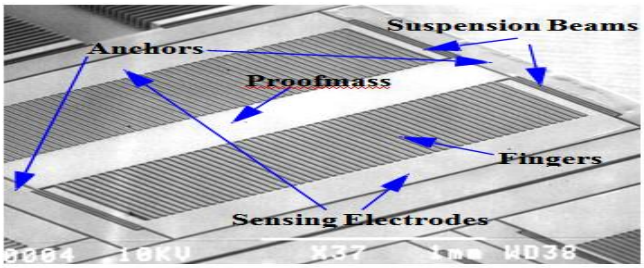


Figure 4. Top view of a MEMS accelerometer.

2.5 CMOS Analog Read-Out Circuits

The detected acceleration, which represents a differential capaci- tance variation from the MEMS accelerometer, is modulated by the analog read-out circuitry shown in Figure 5. In general, the lateral accelerometer presented in Section 2.4 can be operated either in open-loop mode or closed-loop mode. In closed-loop operation the overall performances such as linearity, dynamic range, and band- width are improved [5]. In our design, an electromechanical over- sampled modulator is used because it provides direct digital output and force feedback control of the proof mass simultaneously over a wide dynamic range.

A switched capacitor front-end, shown in Figure 5 (a), was cho- sen because it is insensitive to the input parasitic capacitance. An efficient gain and offset compensated integrator is obtained by using an offset-storage capacitor, C_O, and a correlated double sampling (CDS) technique[7]. This circuit uses a single-ended charge integra- tor to read out the capacitance variation and the static comparator forms the loop quantizer. Finally, a digital flip-flop samples the out- put from the comparator and synchronizes its bit stream with the sys- tem clock. Since the proof mass can be modeled as a second order system the closed loop system becomes unstable so a simple lead compensator, $H_C(z)$, is inserted in the feedback path for stability.

There are four clock phases in the switched-capacitor interface circuit. During the first phase (ϕ_1) the sense capacitors formed

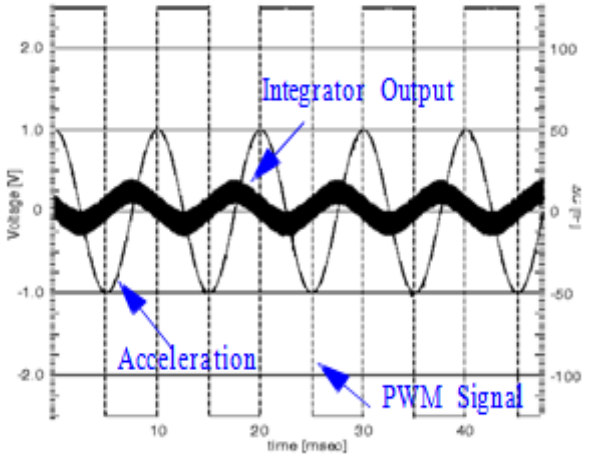


Figure 6. HSPICE simulation for analog read-out circuit.

Between the electrodes and the proof mass are reset and the Op amp offset voltage is stored on C_O. In the second phase (ϕ_2) sense capac- itors, C_{right} and C_{left} are charged through $V+$ and $V-$. The charge dif- ference between C_{right} and C_{left} is integrated on the feedback capacitor, C_i, while the comparator quantizes the charge. In this phase, the offset voltage stored on C_O is substracted and thus the out- put offset voltage of the Op amp is compensated. The amplitude of the Op amp output voltage corresponds to the magnitude of the applied acceleration. For example, if the MEMS device gets positive acceleration, then the proof mass is closer to the left anchor of the MEMS accelerometer and C_{left} is bigger than C_{right}. Since C_{left} is connected to the negative reference voltage ($V-$), the negative net charge is sampled to an integrator, generating a positive Op amp out- put voltage. The capacitance sensitivity defined as the Op amp out- put voltage due to input capacitance change(ΔC) is calculated by:

$$V_{-} = \frac{C}{C_{O}} \left(\right) \qquad (2)$$

From Eqn.(2) the capacitance sensitivity is approximately 0.33 V/pF. The quantized output is also latched at the end of this phase. In the last phase (ϕ_3) the output of the flip-flop is fed back to the MEMS accelerometer to place the proof mass in the nulling position by electrostatic forces. An additional phase (ϕ_4) is used for the con- trol and sensing of the proof mass. The output of the latch forms pulse bit streams for the next module.

Figure 6 shows the HSPICE simulation result of the modulation of acceleration magnitudes into the corresponding digital pulse bit streams (PWM signal). The layout for the analog read-out circuit is shown in Figure 7

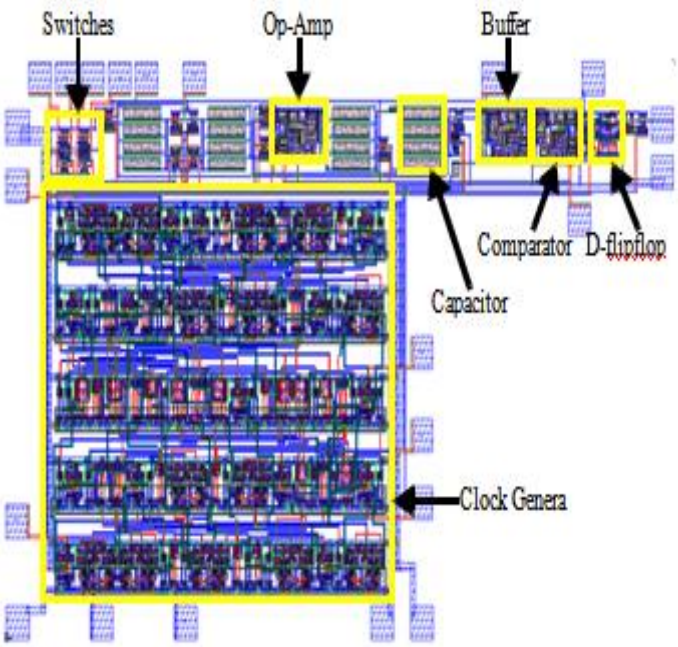


Figure 7. Layout for Sigma-Delta analog readout circuitry,(die size: 4.5mm x 2.6mm)

Higher sampling rates reduce the quantization noise and result in a 3 dB signal-to-noise ratio improvement for each doubling of the sam- pling frequency. Each noise source will now be described.

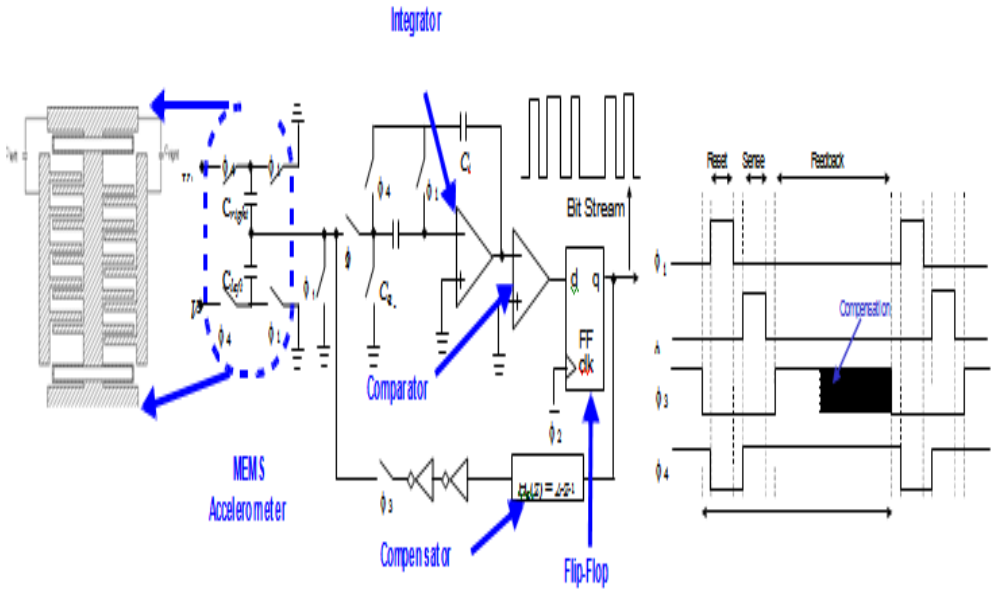
• Brownian noise:

The primary mechanical noise source for the device is due to the Brownian motion of gas molecules between comb fingers. The total noise equivalent acceleration (TNEA)

2.6 Noise Analysis of Closed Loop System

There are several noise sources that affect the performance of the overall system; determining the minimum detectable input accelera- tion. In an oversampled electromechanical sigma-delta system,

where, k_B is the Boltzmann constant, T is the temperature in Kelvin,



is damping coeffiecient, and w_r is resonance frequency. From Eqn.(3), it is seen that the MEMS accelerometer has smaller Brown- ian noise with larger-Q and heavier proof mass. Plugging device data into this equation results in Brownian motion noise around 10
$\sqrt{\mu\gamma}$ Hz

• Amplifier noise:

The readout circuitry utilizes correlated double sampling to reduce the input CMOS amplifier flicker noise; however, the ampli- fier thermal noise is amplified by the ratio of total input capacitors, including parasitics in the integrating capacitor. The noise at the out- put of the amplifier can be expressed by integrating the total noise power and dividing it by the effective noise bandwidth, which is half
the sampling frequency. Therefore, the amplifier output noise volt- age due to thermal noise in the Op amp is expressed as:

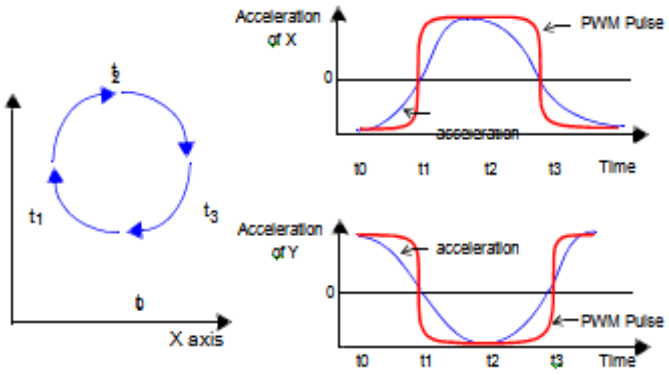


Figure 6. Movements of a mouse and corresponding accelerations in X- and Y-axis.

$$v_{Amp-out} = \sqrt{\frac{16}{3}\frac{C_T}{C_{out}}\frac{kT}{C_{out}}\frac{1}{f_s}} \quad V/\sqrt{Hz} \qquad (4)$$

Where C_T is the total input capacitance including parasitics, C_{out} is the capacitance of the Op amp output node, and f_s is the sampling frequency. From this equation, the equivalent input acceleration noise due to amplifier thermal noise is about 0.7 μ g Hz

And magnitude The polarity indicates the direction of acceleration,

$$a_{n-out} = \sqrt{\frac{kT}{C}}\frac{1}{f_s} \qquad (5)$$

This KT/C voltage noise is converted to equivalent input acceleration noise as 0.3 μ g Hz

And can be handily extracted by observing the sign of pulse bit
where C_T is the total input capacitance including parasitics, C_{out} is the capacitance of the Op amp output node, and f_S is the sampling frequency. From this equation, the equivalent input acceleration noise due to amplifier thermal noise is about 0.7 μ g Hz

• *KT/C* noise:

A major noise source in switched capacitor circuits is *KT/C* noise which is generated by the CMOS switch thermal noise. The rms voltage noise from thermal switch noise can be calculated by the integration of the bandwidth of the switch's RC filter. The voltage noise power density due to this switch thermal noise is expressed as:

Streams. For example, Figure 8 illustrates the movements of the mouse and corresponding acceleration values on both the X- and the Y-axis. It also shows the possible PWM (Pulse Width Modulation) bit streams. If the value of the pulse is 5 volts (digital value "1"), the acceleration is toward the positive direction, and vice versa. The width of the pulse bit streams is proportional to the magnitude of acceleration. The extraction of correct magnitude of acceleration can be achieved via two binary flags (flip-flops) and a binary counter as shown in Figure 9. The "c" flag is set to the polarity of the current.This *KT/C* voltage noise is converted to equivalent input accelera- tion noise as 0.3 μ *g* *Hz*

• Mass residual motion noise:

The proof mass is being rebalanced by a pulse train and thus it has a residual motion with a small ac amplitude. The amplitude of this motion can be shown [8] to be approximately equal to $\Delta x = 4\, a_{max}/(\Delta f_S)^2 = 8.0\text{x}10^{-9}$[m] with a_{max}=20g and f_S=100kHz. This residual motion corresponds to an equivalent rms of 78 mg acceleration in this MEMS accelerometer. This acceleration can be randomized due to the varying input and hence it can be considered to be noise dis- tributed uniformly from dc to the proof mass residual motion fre- quency $f_S/4$. This noise is then equivalent to 500 μ *g* *Hz*

• Dead Zone Noise:

Assuming that the input of the accelerometer is zero, the feed- back voltage generates a_{max} with frequency $f_S/4$ because of electro- static force. Therefore, the input signal must be large enough to break this dead-zone pattern. The minimum rms input acceleration for this is $a_{dead\text{-}zone} = 8a_{max}(f_r/f_S)^2 = 160$ g, and should be counted as noise.

• Total noise and Minimum detectable acceleration:

Since all of the noise sources considered here are uncorrelated

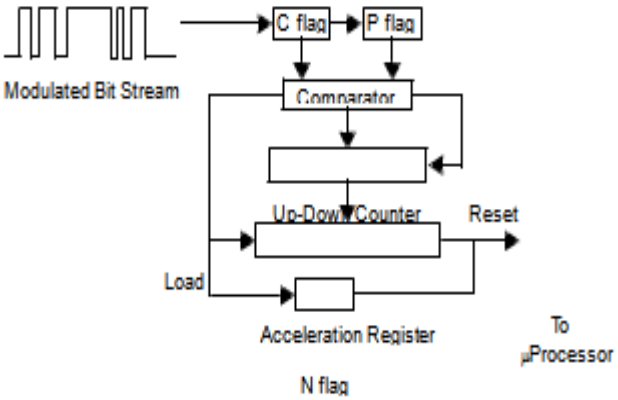


Figure 9. Acceleration Magnitude Extractor.

Input pulse bit stream synchronized by the system clock while the "p" flag value is the one shifted from the "c" flag flip-flop in the pre- vious clock cycle. The comparator compares the two flag values and whenever two flag values differ—i.e. the polarity of the input stream changes—it loads the current value of the binary counter into the"acceleration register" and at the same time resets the counter. While the "c" and "p" flags have the same value, the counter keeps increas- ing or decreasing based on the value of the "c" flag. Thus, the mag- nitude of generated values is proportional to the degree of the acceleration of movements, and the polarity of the input bit steams determines the direction of the user's movements. The positive value of the counter corresponds to positive acceleration and vice-versa. The "acceleration register" always keeps some static values specify- ing the previous acceleration magnitude and the control micropro- cessor only accesses this register to calculate the current position of the cursor. Whenever the acceleration register loads a new value from the counter, the "n" flag is set to "1" indicating that the new they may be summed giving a total noise of 530 μ ⁄ . Thug H zere- value has been loaded. The control microprocessor keeps polling "n" fore, the minimum detectable acceleration is the same as the one cal- culated by integrating this input acceleration density over the bandwidth of interest, ~100 Hz. The resultant minimum detectable acceleration is 5.3 mg, which is below the smallest acceleration a

human hand can generate/perceive. From the noise source consider- ation, we see that the mass residual noise dominates with order of magnitude. However, this mass residual motion noise can be signif- icantly reduced by increasing the sampling frequency at the cost of power consumption and complexity Instruction fetch takes place during the half cycle before the instruc- register value to 16 bit output pins SOUT[15:0]) allowing us to observe any arbitrary register values of the register file during the testing mode. These hardware features provide ways of testing the ROM, RAM, internal registers, and logic circuits.

III. DESIGN STATISTICS

The MEMS accelerometer was designed to have a sensitivity of 0.78 pF/g with dimensions of 2.1mm x 2.4mm x 100 □m (W x L x H) and a sensing capacitance of 16.4 pF. The analog circuit has esti- mated power of 3 mW, capacitance sensitivity of 0.3 V/pF, and diesize of 4.5mm x 2.6mm. Mechanical and analog simulation shows that the designed padless mouse system can detect acceleration as small as 5.3 mg, which is a high enough resolution for mouse appli- cations.

The microprocessor, as shown in Figure 11, contains 53,634 and

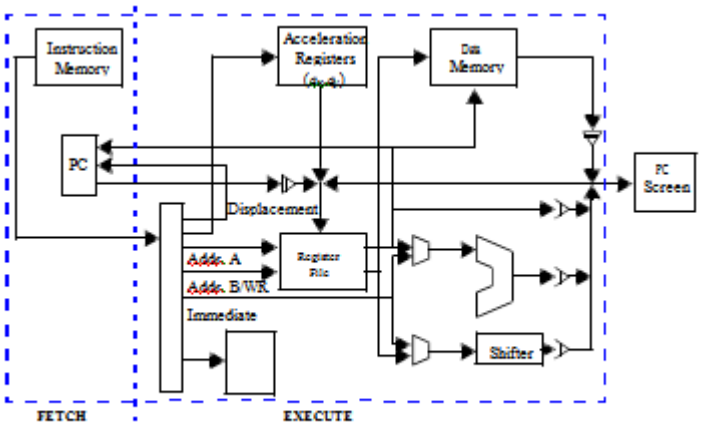


Figure 10. Core microprocessor architecture.

Tion is decoded to allow a full half-cycle for instruction memory access and a full cycle for decoding the instruction. The micropro- cessor uses a 16-bit word and address space and all instructions are single word. In addition to the basic arithmetic and logic operations, two application specific instructions are implemented which will be described below.

The main part of the application program consists of two proce- dures: polling and integration. For the polling procedure, a special instruction is defined called LCNT (Load Counter Value). Which causes the microprocessor to examine the value of the "n" flag in the previous acceleration extract module. If the value of "n" is "1", the contents of the acceleration register are transferred into one of the registers in the datapath module which will be integrated for coordi- nate calculation. At the same time, the "n" flag is reset to "0" by the microprocessor to indicate the completion of the transfer.

The transferred acceleration magnitude value should be inte- grated twice so that it is transformed into position coordinates as shown in the following equation: the die size is 5.6 mm by 5.8 mm. The paths from the register file to ALU were determined to be critical because of a large register file and ripple-carry adder in the ALU. Critical path studies show a max- imum clock frequency of approximately 18 MHz, which is well above the target frequency of 100 kHz. Although maximum achiev- able clock speed is 18.1 MHz, its operation frequency is same as the sampling frequency of the analog switched capacitor sigma-delta read-out circuits. The power consumption is estimated as 10 □W at 100 kHz operation frequency.

IV. MONOLITHIC IMPLEMENTATION

The hybrid two dimensional position detection systems has been proposed to combine MEMS accelerometers and digital circuits by means of switched capacitor circuits using wire bonding. Due to the wire bonding, however, these different modules in a system must interface with each other at board level. This not only limits the size of a system, but also contributes capacitive or resistive parasitics that may degrade the system performance [10]. To circumvent these drawbacks of a hybrid system, a system-on-chip (SoC) design and fabrication, where all the modules are fabricated in single wafer, are considered as a monolithic implementation. In other words, all the necessary modules such as MEMS accelerometers, the analog read- out circuit and the

microprocessor are to be integrated on the same

$$\int_{t_1}^{t} a(t)\,dt = v(t) - v(t_1) \qquad (6)$$

Where v, a, p Represent velocity, acceleration and position coordinate respectively. The integration is performed via two normal addition Instructions: $v \leftarrow v + a$ and $p \leftarrow p + v$. Since the system has abun-

Wafer without any interfaces between them. The only major inter- face with outside circuits -other than VDD, GND, clock and reset

$$\int_{t_1}^{t} a(t)\,dt = v(t) - v(t_1)$$

Where v *a p*,

Represent velocity, acceleration and position coordinate respectively. The integration is performed via two normal addition instructions: *v* ← *v* + and *p* ← *p* + . Since the system has abun- dant instruction cycles per coordinate calculation as pointed out in Section 2.1, the lack of special purpose hardware is justified.

The other special instruction is called SROUT which moves cal- culated coordinate values to the 16-bit system interface bus. To min- imize the interface with outside circuitry, instruction memory (ROM) as well as data memory (RAM) have been integrated into the core microprocessor module. Both ROM and RAM are 256 words which, due to the simplicity of application program, is big enough to contain the entire application program.

V. VERIFICATION AND TESTING

Verification and simulation were performed using the Mentor Graphics Tools and Epoch Design Compiler. Mentor's Quicksim Pro was used for transistor level and Verilog simulation. Parasitics were extracted from the layout, and Mentor's Accusim used for the detailed delay and loading effects. Timing information from the parts generated in Epoch [9] was extracted automatically during the import process to Mentor's Design Architect. Once the functional models were properly back annotated, timing verification was per- formed in Quicksim Pro. In order to verify the physical design, full mask LVS was performed by importing the custom datapath into Epoch and generating a netlist for the entire core that included the custom and Epoch-synthesized parts. To facilitate testing, the program counter and instruction register were made scannable. The instruction SROUT moves the specified.

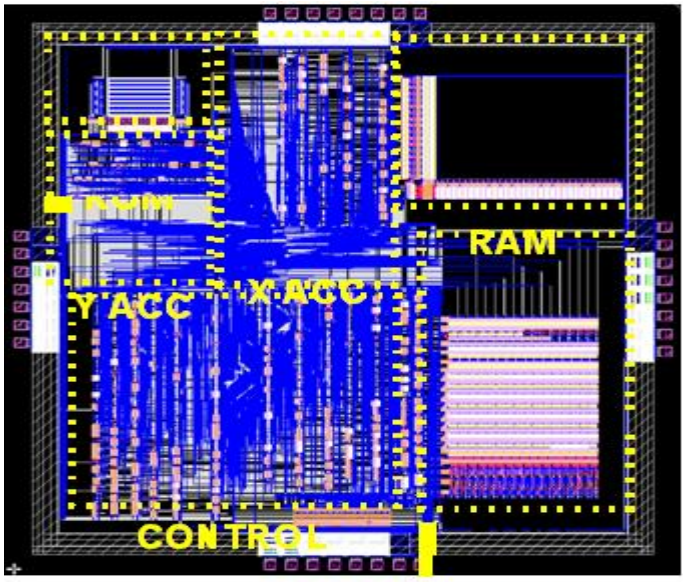


Figure 11. Microprocessor layout. (5.6mm x 5.8mm)

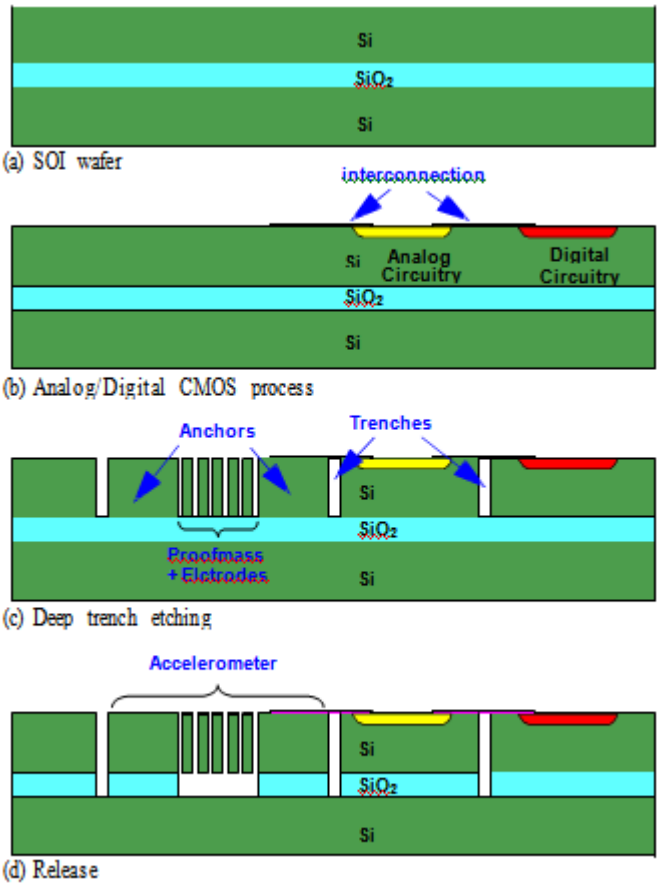


Figure 12. Process flow of monolithic implementation.

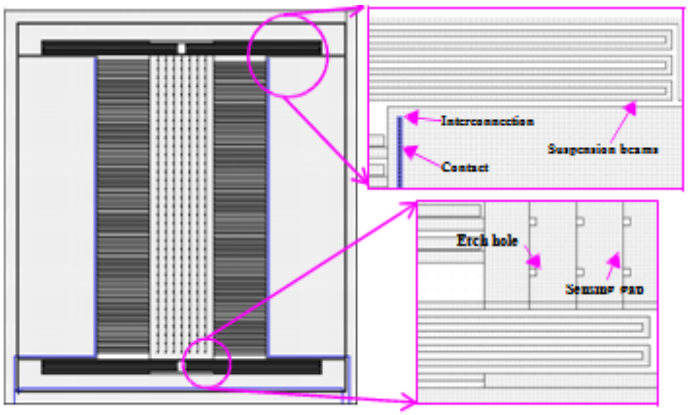


Figure 13. MEMS accelerometer for monolithic

VI. CONCLUSION

In this paper, we presented a novel two-dimensional position detection system for padless mouse applications that do not require any contacts for proper mouse operation. The design requirements were carefully examined and the systematic design methodology was established. The final system consists of four major compo- nents: 1) MEMS accelerometer, 2) Analog read-out circuit, 3) Acceleration magnitude extraction module and 4) 16-bit RISC microprocessor. Each module was carefully designed, laid out, and verified through extensive simulation. The calculated and simulated minimum detectable acceleration is 5.3 mg.

The hybrid multi-chip nature of the proposed system will limit the system size and contribute capacitive and resistive parasitics that may degrade the system performance. To circumvent these draw signals- is the parallel data bus which transfers positional coordi- nates calculated from the microprocessor. Since they are fabricated on the same wafer, it greatly reduces the overall costs as well as com- plex steps for the interface. With all these advantages over hybrid system, however, monolithic system has several problems such as noise between analog

and digital circuits, interconnections between MEMS devices and analog circuits, and so on. One of the main factor for a noise problem in a monolithic system stems from the fact that the analog and digital circuits are sharing the same substrate. Although substrate has high resistance, it is not a complete isolator and thus voltage variations in digital parts are capacitively coupled to analog circuits and thus may cause malfunctions of a system.

This noise problem due to the substrate coupling can be solved by using Silicon-on-Insulator (SOI) which isolates one module from the other by etching the substrate boundaries of each module and making it isolated both physically and electrically. And more, MEMS accelerometers and analog circuitry can be connected to each other by making deep trenches. It is reported that the silicon substrate underneath interconnection materials such as metals can be removed in the process of deep trench etching because of a sidewall etching effect [11]. The detailed fabrication process flow for mono- lithic implementation combining MEMS devices, analog and digital circuits are basically post CMOS fabrication, presented in Figure 12. The usual CMOS processes are done using SOI start-wafer as shown in Figure 12(a) and (b). After CMOS processes, deep trenches are made for the formation of proofmass of MEMS accelerometer as well as isolation between analog and digital circuitry as given in Fig- ure 12(c). Figure 12(d) presents the release step by removing SiO_2 with BHF to suspend the proofmass. During release, the SiO2 between analog/digital circuitry are also etched away. Figure 13 shows the mask level MEMS structure. Close-up view shows a inter- connection line, contacts, suspension beams, and etch holes which help releasing proofmass during BHF etch process. Backs, a system-on-chip (SoC) design and fabrication, where all the modules are fabricated on a single wafer, are considered as future work in this area. Also, the system can be handily extended into a three-dimensional position detection system by adding an additional MEMS accelerometer to measure *Z*-axis directional movement.

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