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Design of Stepped Impedance Microstrip Low Pass Filter with DGS

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Abstract:- A design of Butterworth stepped impedance microstrip low pass filter with DGS is presented in this paper. Two designs are introduced. The first design is a seven order low pass filter with three interdigital slots with different finger lengths inserted under the position of high impedance lines. The maximum insertion loss in the passband is better than 0.97 dB and the maximum group delay variation within the passband is less than 10 ps. The other design is a nine order low pass filter that use different shapes of the DGS (rectangular, square dumbbell and interdigital). The maximum insertion loss is about 0.5 dB and maximum group delay variation is 27 ps. The cutoff frequency of the proposed two designs is 16 GHz. The filter used for LEO satellite application. The filter is analysed using CST Microwave Studio, IE3D zeland and ADS. The filter is fabricated with photolithographic technique and scattering parameters are measured by using Vector Network Analyzer. Measurements and simulations show good agreement.

Keywords:-Stepped impedance, LPF, DGS, interdigital, dumpbell.

I. INTRODUCTION

Filters play an important role in microwave communications and are used to pass or eliminate specific frequency bands. Filters are classified as low-pass (LP), high-pass (HP), band-pass (BP), and band-stop (BS). LPF is used at the output of a power amplifier to eliminate the harmonics generated by the nonlinearity of the power amplifier, at the output of a mixer to pass only the intermediate frequency, at the input of a receiver to reject the unwanted higher frequencies and in conjunction with a HPF to realize a wideband band-pass filter.
Microwave filters can be divided into two main different types, lumped or distributed. Lumped elements consist of discrete elements, such as inductors and capacitors, while distributed elements use the lengths and widths of transmission lines to create their inductive or capacitive values [1].

Microstrip line is a good candidate for filter design due to its advantages of low cost, compact size, light weight, planar structure and easy integration with other components on a single board. To achieve better performance for the microwave filters, such as increasing steepness of the cut-off slop, and to increase the stopband range of the microwave filters, defected ground structures (DGS) are used. This technique is realized by etching slots in the ground plane of the microwave circuit. This technique is used for microstrip and coplanar waveguide transmission lines [2-6].

In section II, DGS LPF design concept is illustrated. Implementation and measurement DGS LPF are presented in section III. While, the paper conclusion is given in section V.

II. DGS-LPF DESIGN CONCEPT

To construct specific filters using the insertion loss method, we'd like to be able to relate the desired frequency characteristics to the parameters of the filter structure. The general filter design flow by insertion loss method is shown in fig.1.

First of all, the required filter specifications should be characterized, for example, low-pass, high-pass or band-pass filter, required cut-off frequency, cut-off rate and passband characteristics, etc. Then choose the required response to be used, maximally flat response or equal ripple, etc. The proposed filter is a seven and nine order maximally flat LPF with cut-off frequency of 16 GHz.
The second step is to design the low-pass prototype. For Butterworth response the specific formula to determine prototype values as shown in fig.2 [7]. This formula is

$$g_0 = g_{n+1} = 1 \quad (1)$$

$$g_i = 2\sin\left[\frac{(2i-1)}{2n}\right]; i = 1, 2, \ldots \ldots . n \qquad (2)$$

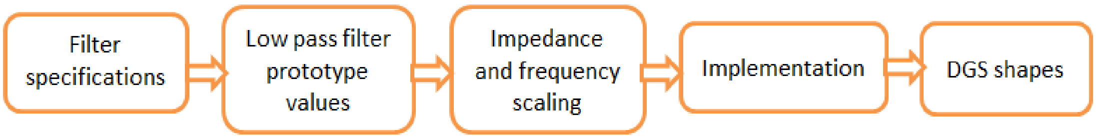


Fig.1: DGS Microstrip filter design steps

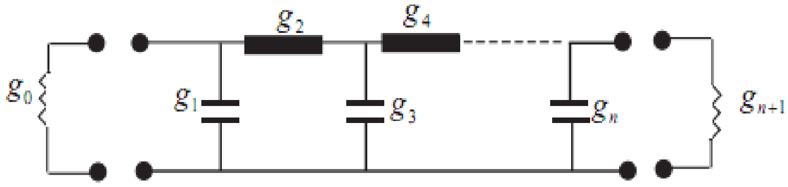


Fig.2: Odd order low-pass prototype filter

The third step in the design process is to shift the prototype response to the required frequency, i.e. frequency scaling, then apply impedance scaling for better matching.

Formula to calculate L_i and C_i

$L_i = \frac{g_i Z_0}{w_c}$ (3)

$C_i = \frac{g_i}{Z_0 w_c}$ (4)

The fourth step in the design process is to convert all the lumped elements to distributed elements using certain transformations. The proposed LPF is stepped-impedance low-pass microstrip filters, which use a cascaded structure of alternating low and high impedance transmission lines. The low impedance lines act as shunt capacitors and the high impedance lines act as series inductors [8].

The filter is fabricated using RT/duroid 5880 substrate with parameters of dielectric constant ε_r =2.2, thickness h=1.575 mm and loss tangent tan δ =0.0009.

The electrical length of capacitor section

$\beta l = \frac{g_i * Z_L}{Z_0}$ (7)

The electrical length of inductor section

$\beta l = \frac{g_i * Z_0}{Z_h}$ (6)

Those lengths should be evaluated at $\omega = \omega_c$.

The last step of the design procedures is to make the suitable DGS. There are various shapes of DGS as shown in fig.3 [9].The shapes of DGS used in the proposed LPF are interdigital, rectangular and dumpbell with square head slots.

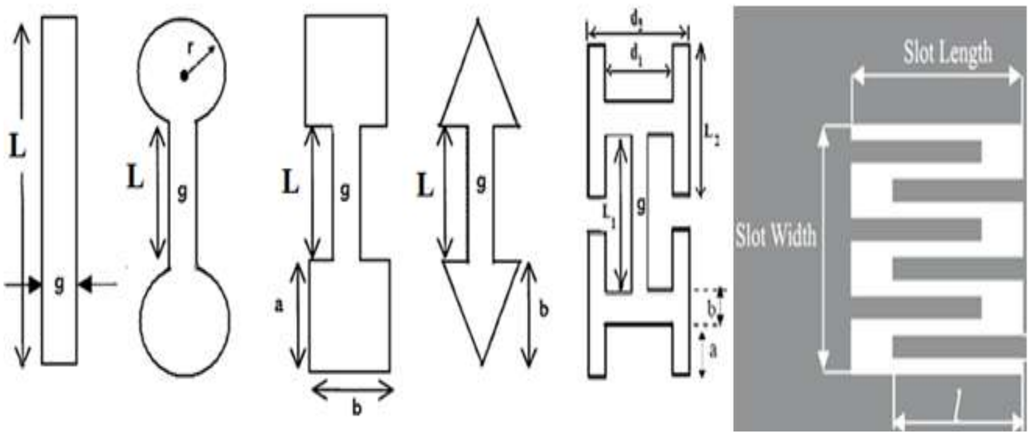


Fig.3: Different DGS slots. These are rectangular, circular head, square head, arrow head, H-shape head and interdigital defects (from left to right) [9].

III. IMPLEMENTATION AND MEASUREMENT DGS LPF

A. A seven order maximally flat LPF

A.1. A seven order LPF without DGS

Table I: Prototype filter elements and ideal circuit elements of a seven order Butterworth LPF.

Item	g_i	Circuit element	Value	Unit
0, 8	1	Z0, Z8	50	Ω
1, 7	0.445	C1, C7	0.08853	Pf
2, 6	1.247	L2, L6	0.62021	nH
3, 5	1.8019	C3, C5	0.35848	Pf
4	2	L4	0.99472	nH

By substituting all these L and C values in the network design, we have the circuit shown in fig.4.

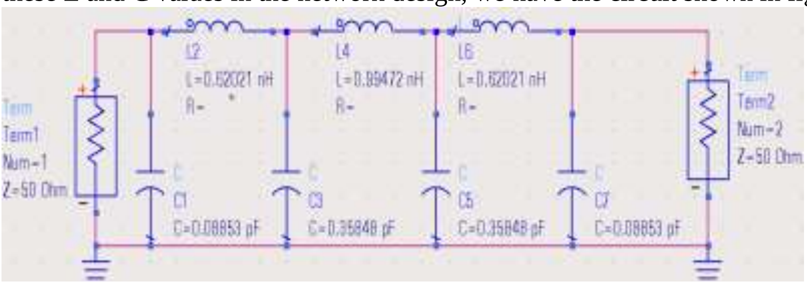


Fig.4: lumped element seven order LPF Output waveform of lumped elements seven order LPF using ADS simulator is shown in fig.5.

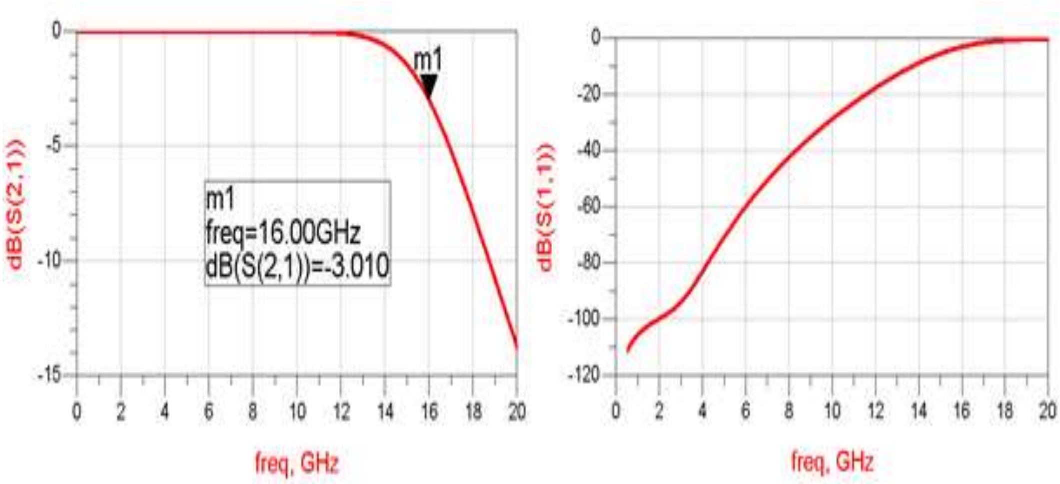


Fig.5: S-parameters of lumped element seven order LPF

Using Z_h = 70 Ω and Z_L = 43 Ω, the capacitive and inductive elements of the filter are realized by sections of low and high impedance transmission lines as shown in fig.6.

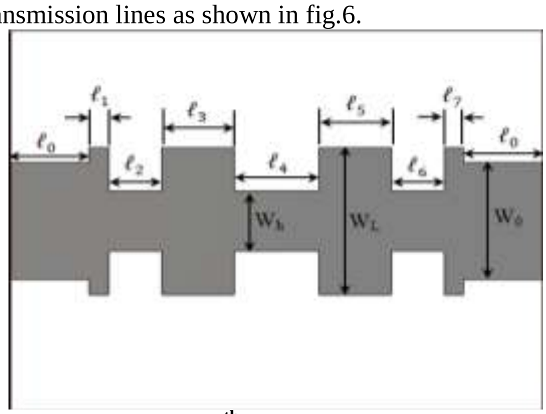


Fig.6: The structure of 7th order stepped-impedance LPF. The lengths and widths are showing in tables II and III.

Table II

Length	L_0	L_1 , L_7	L_2 , L_6	L_3 , L_5	L_4
Values (mm)	**3**	**0.75**	**2.02**	**2.77**	**3.25**

Table III

Width	W_0	W_L	W_h
Value (mm)	4.9	6.3	2.6

Where W_0 corresponds to the 50 Ω impedance at input and output.
W_L corresponds to the low impedance Z_L.
W_h corresponds to the high impedance Z_h.

The comparison between simulation results using different simulation programs (CST, Zeland and Momentum ADS) of 7th order LPF without DGS are shown in fig. 7.

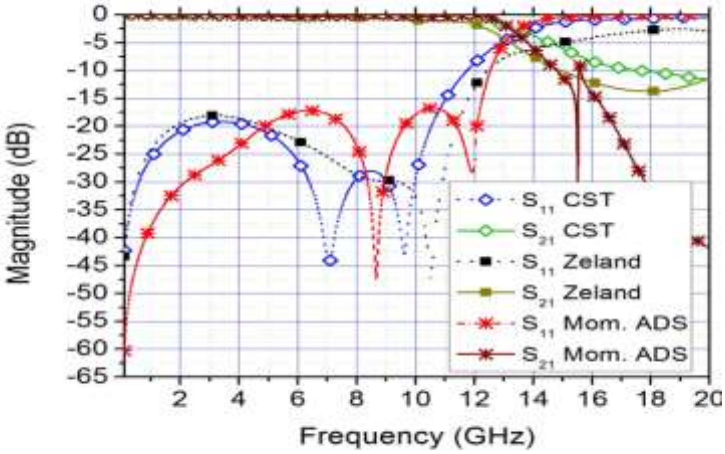


Fig. 7. Simulated S-parameters of seven order stepped impedance LPF without DGS.

A.2. A seven order LPF with DGS

By using three interdigital slots are inserted under the position of high impedance lines as shown in fig. 8.

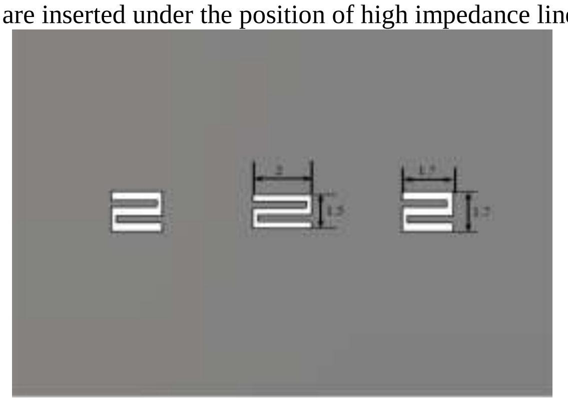


Fig. 8: The back side of seven order stepped impedance LPF with DGS

The Photograph of the fabricated seven order LPF with DGSis shown in fig. 9.

(a) (b)

Fig. 9: Photograph of the fabricated 7th order LPF. a) top side b) bottom side

The simulated and measured insertion and return loss of the filter is shown in fig. 10.

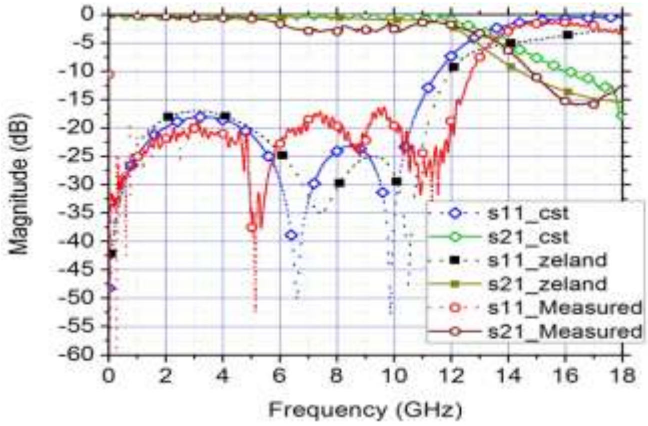


Fig. 10: Performances of the seven LPF with DGS

The simulated and measured group delay of the filter shown in fig. 11.

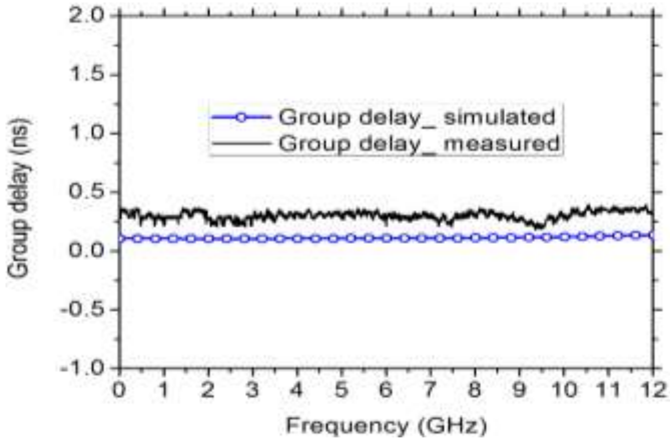


Fig. 11: Group delay of the seven LPF with DGS.

B. A nine order maximally flat LPF

B.1. A nine order LPF without DGS

Table IV: Prototype filter elements and ideal circuit elements of a nine order Butterworth LPF.

Item	g_i	Circuit element	value	Unit
0 , 10	1	Z0 , Z10	50	Ω
1 , 9	0.3473	C1 , C9	0.0691	Pf
2 , 8	1	L2 , L8	0.49746	nH
3 , 7	1.5321	C3 , C7	0.3048	Pf
4 , 6	1.8794	L4 , L6	0.93474	nH
5	2	C5	0.3979	Pf

By substituting all these L and C values in the network design, we have shown in fig. 12.

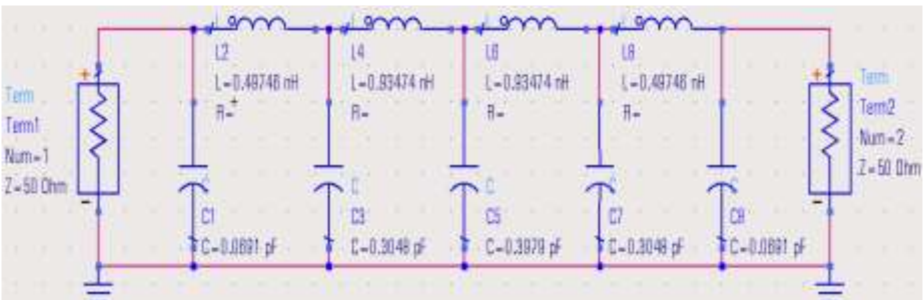


Fig. 12: Lumped element nine order LPF.

Output waveform of lumped elements nine order LPF using ADS simulator is shown in fig. 13.

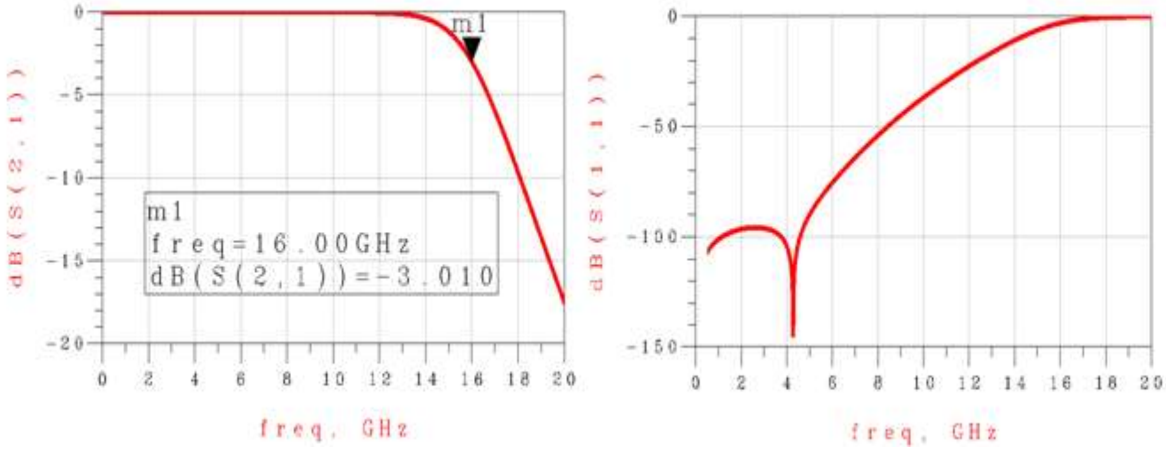


Fig. 13: S-parameters of lumped element nine order LPF.

Using $Z_h = 72\ \Omega$ and $Z_l = 39\ \Omega$, the capacitive and inductive elements of the filter are realized by sections of low and high impedance transmission lines as shown in fig. 14.

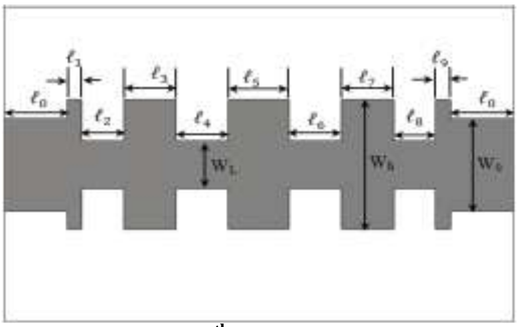


Fig.14: The structure of 9th order stepped-impedance LPF.

The lengths and widths are showing in tables V and VI.

Table V

Length	L_0	L_1 , L_9	L_2 , L_8	L_3 , L_7	L_4 , L_6	L_5
Values (mm)	3	0.7	2	2.5	2.5	2.9

Table VI

Width	W_0	W_L	W_h
Value (mm)	4.9	7	2.6

The comparison between simulation results using different simulation programs (CST, Zeland and Momentum ADS) of 9th order LPF without DGS are shown in fig. 15.

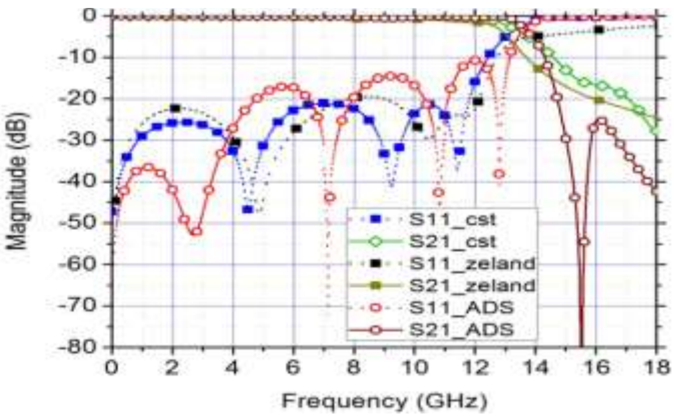


Fig. 15: Simulated S-parameters of a nine order stepped impedance LPF without DGS.

B.2. A nine order LPF with DGS

1. Using two similar dumbbells with square head and two similar interdigital slots are inserted under the position of high impedance lines as shown in fig. 16.

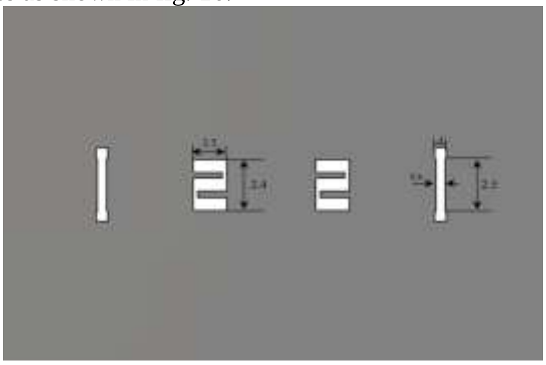


Fig. 16: The back side of a nine order stepped impedance LPF with DGS1.

The simulated S-parameters of the filter are shown in fig. 17.

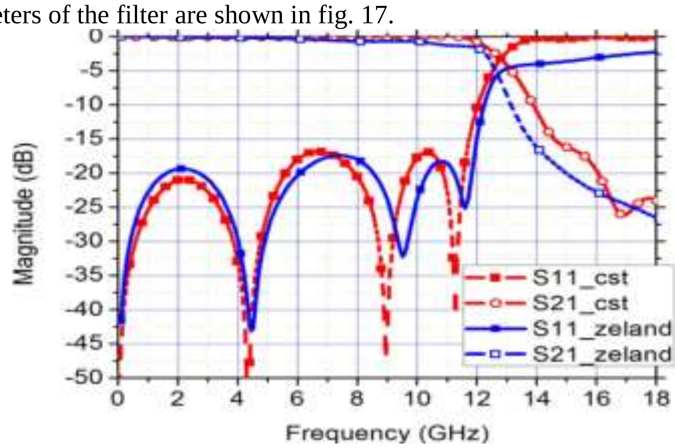


Fig. 17: Simulated S-parameters of a nine order stepped impedance LPF with DGS1.

2. Using two similar interdigital slots and two similar rectangular slots as shown in fig. 18.

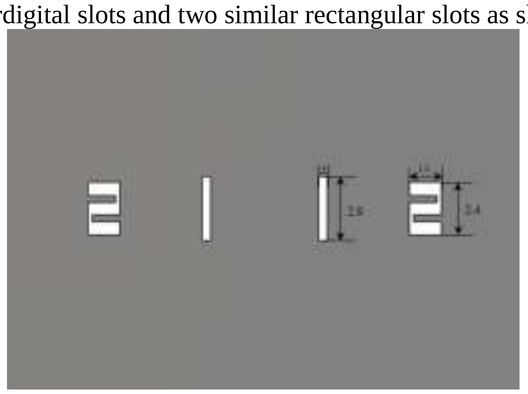


Fig. 18: The back side of a nine order stepped impedance LPF with DGS2.

The simulated S-parameters of the filter are shown in fig. 19.

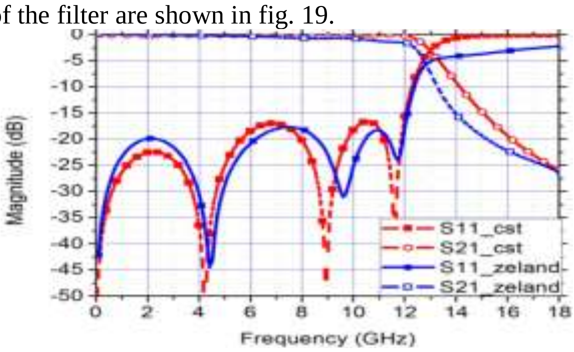


Fig. 19:Simulated S-parameters of a nine order stepped impedance LPF with DGS2.

3. Using four interdigital slots as shown in fig. 20.

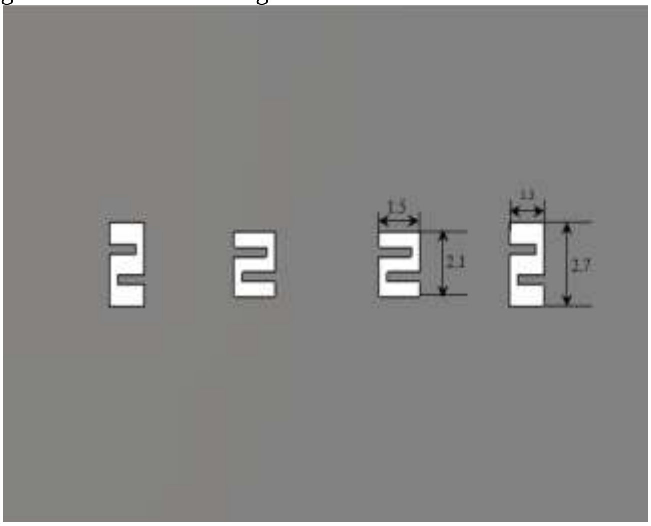
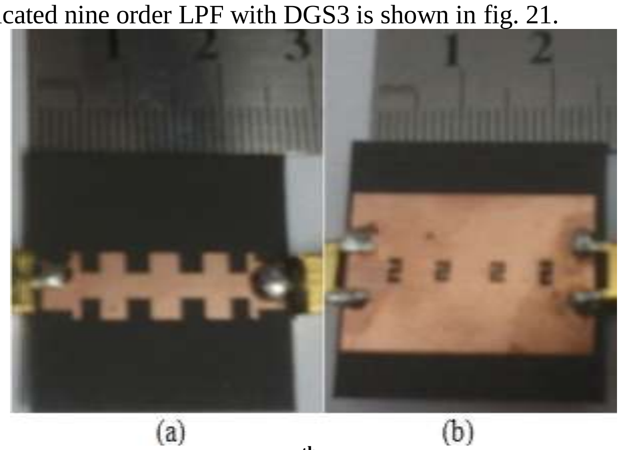


Fig. 20: The back side of a nine order stepped impedance LPF with DGS3.

The Photograph of the fabricated nine order LPF with DGS3 is shown in fig. 21.



(a) (b)

Fig. 21: Photograph of the fabricated 9th order LPF. a) Top side b) bottom side

The simulated and measured insertion and return loss of a nine order LPF with DGS3 is shown in fig. 22.

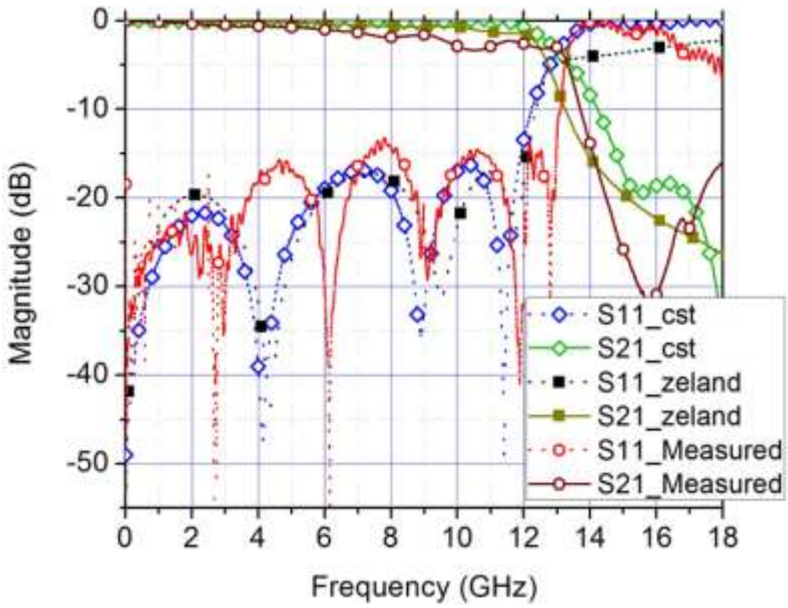


Fig..22: The simulated and measured insertion and return loss of a nine order LPF with DGS3.

The simulated and measured group delay of the filter shown in fig. 23.

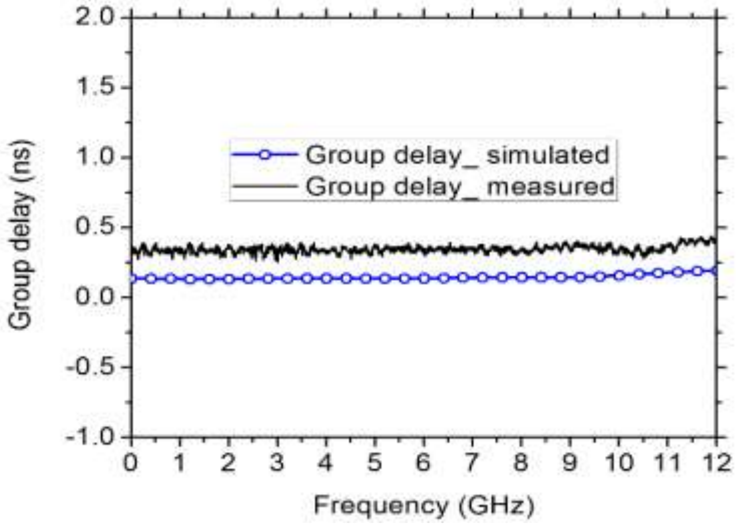


Fig. 23: Group delay of the nine LPF with DGS3.

Table VII Summarizes the performance of the proposed LPF.

Table VII: Summary of LPF

Filter order	DGS shapes	IL at 8 GHz	IL at 12 GHz	Group delay(ps)	Size
7th	--------	0.8	-8	117 ±8	20.33 * 6.3
7th	Interdigital	0.97	-10	122 ± 11	20.33 * 6.3
9th	--------	0.24	-16	162 ± 22	24.3 * 7
9th	Rectangular, interdigital	0.2	-20	171 ± 32	24.3 * 7
9th	Dumpbell, interdigital	0.8	-20	175 ± 28	24.3 * 7
9th	Interdigital	0.5	-18	172 ± 27	24.3* 7

IV. CONCLUSIONS

In this paper, seven and nine order stepped impedance DGS LPF are proposed. For the first design seven orders DGS LPF, the maximum insertion loss in the passband is better than 0.97 dB and the maximum group delay variation within the pass band is less than 10 ps and has small size of (20.33 * 6.3) mm2. The second design is a nine order DGS LPF, the maximum insertion loss is about 0.5 dB and maximum group delay variation is 27 ps and has small size (24.3 * 7) mm2. The proposed compact and high performance LPF can be broadly used to reject higher harmonics and spurious response for wideband microstrip circuits and systems applications.

REFERENCES

[1]. Ms.Vandana M. Anerao, “Implementation of Stepped Impedance Microstrip Low Pass Filter,’’ International Journal of Emerging Trends in Electrical and Electronics (IJETEE), Vol. 2, Issue. 2, April-2013.

[2]. M. CHALLAL, A. AZRAR, and D. VANHOENACKER JANVIER, “A Novel Ultra-Wide Stopband Microstrip Low-Pass Filter for Rejecting High Order Harmonics and Spurious Response,’’ 24th International Conference on Microelectronics (ICM) IEEE, 2012.

[3]. D. Ahn, J. S. Park, C. S. Kim, Y. Qian, and T. Itoh, “A Design of the low-pass filter using the novel microstrip defected ground structure, ” IEEE Trans. Microw. Theory Tech.,vol. 49, pp.86-91, 2001.

[4]. H. J. Chen, T. H. Huang, C. S. Chang, L. S. Chen, N. F. Wang,Y. H Wang, M. P. Houng, “A novel cross-shaped DGS applied to design ultra-wide stop-band low-pass filters,” IEEE Microw. Wireless Comp. Lett.,vol. 16, no. 5, pp. 252–254, May 2006.

[5]. S. W. Ting, K.W. Tam, and R.P. Martins, “Miniaturized microstrip lowpass filter with wide stop-band using double equilateral u-shaped defected ground structure, ”IEEE Microw. Wireless Compon Lett.,vol.16, pp. 240–242, May 2006.

[6]. P. Y. Hsiao, R. M. Weng, “An ultra-wide stop-band low-pass filter using dual reverse U-shaped DGS”, Microw. and Optical Technology Lett., vol. 50, no. 11, pp. 2783-2780, November 2008.

[7]. K.Rajasekaran, J.Jayalakshmi and T.Jayasankar, “Design and Analysis of Stepped Impedance Microstrip Low Pass Filter Using ADS Simulation Tool for Wireless Applications,” International Journal of Scientific and Research Publications, Volume 3, Issue 8, August 2013.

[8]. D. M. Pozar,’’ Microwave Engineering,’’ Fourth edition, John Wiley&Sons Inc.,2012.

[9]. Doktoringenieur, ‘’Analysis, Design, Optimization and Realization of Compact High Performance Printed RF Filters,” 2010.