A 8-bit high speed ADC using Intel µP 8085

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Abstract:- An 8-bit ADC Architecture of is proposed, it uses 16 comparators and produces 8-bit digital code in half the time as that of successive approximation technique. In this approach, the analog input range is partitioned into 16 quantization cells, separated by 15 boundary points. A 4-bit binary code 0000 to 1111 is assigned to each cell. The results show that the ADC exhibits a maximum DNL of 0.49LSB and a maximum INL of 0.51LSB.

Keywords:- ADC, Microprocessor, DAC, Sample and Hold. Successive approximation.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2^{N-1} comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2].

All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially, and consequently this architecture requires very large IC's. It has high power dissipation. Two step Flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [3, 4]. However, beyond such resolution, the area and power dissipation of two-step Flash ADC's nearly double for each additional bit of resolution [5].

Typically high-resolution ADC's have been based either on self-calibrated successive approximation [6,7] or over sampling architectures [8, 9]. But both of these architectures are unsuitable for high speed applications.

There are many different architectures like pipelined convertor [10, 11], successive approximation convertor [12, 13], Sigma-Delta convertor [14], folding ADC's [15], reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper an 8-bit Architecture of analog-to-digital (A/D) converter is proposed to improve the sampling rate of an ADC. The prototype ADC based on this technique uses only 17 comparators and needs only four comparisons, instead of eight comparisons normally required in the conventional successive approximation techniques for 8-bit resolution. This can increase the speed of conversion.

II. ADC ARCHITECTURE

The block diagram of the proposed 8-bit ADC is illustrated in Figure-1. It is based on a conventional successive approximation technique. The ADC consists of an input sample and hold amplifier (SHA), 4-bit flash ADC, 8-bit DAC, 8-bit µP 8085 and some extra supporting circuit blocks. 4-bit flash ADC partitions input range into 16-quantization cells. From the 4-bit code µP8085 decides within which cell the input sample lies. This gives 4 MSB bits 0000 to 1111 according to the cell value. Remaining 4 bits are obtained by successive approximation technique.

A binary count is loaded into the Register A depending on the 4-bit code. The detailed binary count to be loaded for different code is summarized in table-1.
The Analog to digital converter is designed and developed using µP8085.
The 4-bit code generated by 4-bit flash ADC is fed to Port A of 8255. Depending on the code value, a binary count is loaded in Register A as given in table -1. The successive approximation technique is used to get a final 8-bit digital code for the analog input signal.
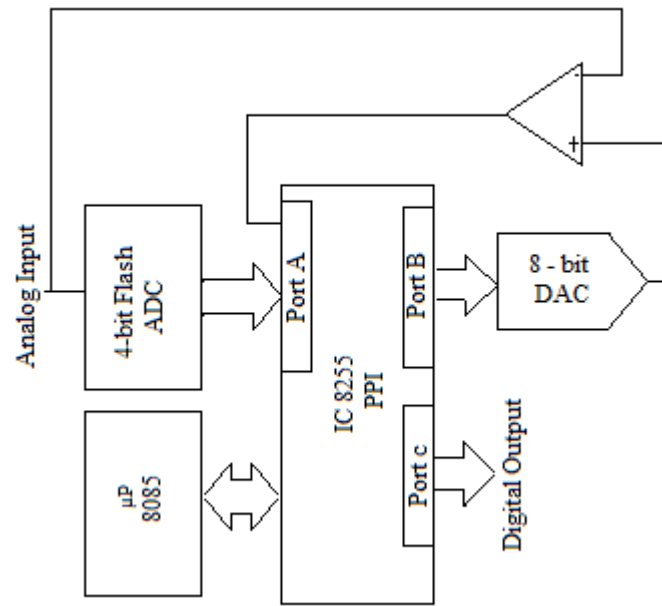
Figure 1: Block Diagram of 8-bit ADC

Table 1: Binary count corresponding to thermometer code

Thermometer code	Count to be loaded in to the accumulator
0000H	08H
0001H	18H
0002H	28H
003H	38H
0004H	48H
0005H	58H
0006H	68H
0007H	78H
0008H	88H
0009H	98H
000AH	A8H
000BH	B8H
000CH	C8H
000DH	D8H
000EH	E8H
000FH	F8H

III.   CIRCUIT IMPLEMENTATION

The block diagram of the 8-bit ADC is as shown in Figure 1. The 8255 port A is used as input port which gets the 4-bit code from Flash ADC. Corresponding 8-bit binary code is loaded into the accumulator as in the table-1. Port B is used as output port, connected to 8-bit DAC to obtain analog signal equivalent to digital count in Register A, which is compared with an analog input voltage V_{IN}. Equivalent 8-bit digital code for analog input signal is obtained by successive approximation technique. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, $V_{ref\,(DAC)}$ provided by DAC is set to $V_N / 2$ to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with $V_N/4$ or $3/4*V_N$ depending on the result of the MSB. If the MSB is "1", then $V_{ref(DAC)} = ¾*V_N$, otherwise $V_{ref(DAC)} = V_N/4$. This sequence will continue until the LSB is obtained. After completion of four comparisons, count in the Register A is digital equivalent of Analog input voltage V_{IN}. To get an   8-bit digital output, 4 comparisons are needed, while it is 8

comparisons in the normal successive approximation ADC. Finally 8-bit digital code is available at port C. Software for implementing successive approximation converter in µP8085 is written in assembler code.

IV. MEASURED RESULT

An experimental prototype of 8-bit ADC using proposed technique was designed and developed using µP8085. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 3.5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 255 for 8-bit at the output, indicating that the ADC's working is functionally correct. Both the differential and integral nonlinearities (DNL and INL) were measured over 2^8 output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 255 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.49LSB and a maximum INL of 0.51LSB as shown in the Figures 2(a) and 2(b).
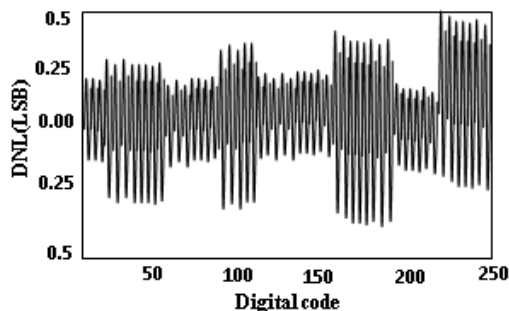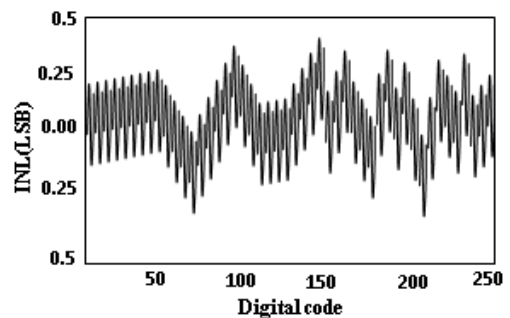
Figure 2(a): DNL Versus output Code   **Figure 2(b): INL Versus output Code**

V. CONCLUSION

We have presented a simple and effective technique for enhancing speed of a successive approximation ADC. This technique would be effective in a large number of high speed controls and signal processing applications such as hard-disk-drive read Chanel and wireless receivers. Although these applications are most often implemented with Flash convertors, but these ADC's demands larger power. Also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10bits. This paper shows that partitioning analog input range increases the conversion rate of successive approximation ADC's. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 10bit resolution.

Implementation of successive approximation algorithm in Microprocessor has reduced the hardware requirement and cost. Proposed technique uses only 16 comparators to enhance speed of 8-bit successive approximation ADC by 50%.

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