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Interconnected Serialized Architecture for Transmission Systems

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Abstract:- Transmission system with proposed multiplexer-flip-flops (MUX-FFs) has a high throughput and low-cost solution for serial link transmitters. MUX-FFs is designed with proposed multiplexer-latches that possess a logic function of various combinational circuits and storing capacity of sequential circuits. Pipeline arrangement with MUX-FFs composed of cascaded latches and MUX-latches with this many latch gates for sequential can be removed. Simulation results show that a 8-to-1 serializer with MUX-FFs reduces 63% gate-count compared to traditional pipeline transmission architecture. The measured results shows that the MUX-FFs and the proposed transmission architecture are almost bit error free and high speed in transmission.

Keywords:- MUX-FFs and MUX-latches, pipelined serializer, gate-count

I. INTRODUCTION

The design techniques for the serial link can be categorized into two groups, the pipeline and non-pipeline topology. The non-pipeline topology has the advantages of low chip area and power while the pipeline topology has the advantages of very high operating speed. The non-pipeline topologies such as the fan-in multiplexer and the tree-topology multiplexer with multiphase clocks have been proposed for low-cost solutions for transmission. The large fan-in multiplexer processes more-than-two input data in a single gate. And in the large fan-in multiplexer, the parasitic capacitance of the output node is large and causes long MUX gate delay. The multiplexer adopts the common number of latch circuit used for implementation. In this project, I am operating up to 12 gigabits/s and I am using 180-nm CMOS technology. And we are using less gate count. Serial link transmitter separates the data transmission of the MUX stages and improves the data throughput.
The pipelined multiplexer implemented with static logic and also a portion of area and power overhead in the serial link circuit. A MUX-FF is composed of cascaded MUX-Latches and latches. In this paper provides detail area and delay analysis of the MUX-FF that performs

Multiplexing and clock-edge-triggered sampling functions like the MUXs and the FFs in the conventional topology. The pipeline behavior of the MUX Latch and clock-edge-triggered sampling function of the MUX-FFs is shown. The function of the smallest unit MUX-FF is a 4-to-1 MUX with clock-edge-triggered sampling is analyzed. A unit MUX-FF saves six latches compared with a conventional pipeline 4-to-1 MUX. With the MUX-FFs, the gate-count of the proposed serializer is reduced significantly as the inputs of the serializer increases. The Tree-topology employs multiphase low-frequency clock signals rather than high-frequency clock signals. Designs achieve area saving through cascaded MUX without pipeline flip-flops (FFs). However, the multiple cascaded MUX stages become critical data paths and that limits the operating speed. Due to this limitation, the pipeline topology is more commonly adopted to achieve high-speed design.

The rest of the paper is organized as follows. A brief overview of related work is offered in section II, a detailed overview of proposed systems and its explanation in section III. Section IV provides the results of proposed systems and conclusions are offered in section V.

II. RELATED WORKS

In this paper [1] "A Novel MUX-FF circuit for low power and high speed serial link interfaces" was proposed by Wei-YU Tsai, Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, Yar-Sun Hsu. In this paper they implemented a MUX- FF by cascading two stages of MUX-Latches but the area and power consumption of a MUX-FF are of 56% and 72% of a conventional MUX.

In this paper [2] "Simulation and Analysis of 2:1 Multiplexer circuit at 90nm technology" was proposed by Ila Gupta, Neha Arora, B.P.Singh. In this paper they represent the simulation of different analysis on different parameters such as Power, Voltage, Frequency, and temperature. In this they use NMOS 2:1 Multiplexer for my implementation of Clock Pulse Generator (CPG) circuit to provide clock-edge-triggered sampling for MUX-Latch circuit. But I am using simple AND gate structure for implementing the clock pulse generator circuit to provide clock-edge-triggered sampling for MUX-Latch circuit.

In this paper [3] "A novel low gate-count pipeline topology with multiplexer-flip-flops for serial link" was proposed by W.-Y. Tsai, C.-T. Chiu, J.-M. Wu, S. S. Hsu. The gate count is more in this paper. And the complexity in design makes the system with less speed and more area and more delay in transmission.

III. PROPOSED SYSTEM

There are three clock signals CLK, CLKH, and CLKHH and four control signals P0, P1, P0H, and P1H**.** The frequency of CLK is two and four times of that of CLKH and CLKHH. The frequency of P0 and P1 is half of that of CLK and P0/P1 are 25% duty cycle pulse signals. In the first input stage, the CLKHH in the latches is used to pre-sample the data of INPUT 2 and INPUT 3 and hold for half period. The data INPUT 2 and INPUT 3 from NODE 1 and NODE 2 is held for half-period in terms of CLKH. Similarly, the CLKH is providing phase delay of half period to NODE 4. In the MUX-Latches, the propagations are controlled by P0H/P1H and P0/P1, and the holding periods are controlled by CLKH and CLK .The gate count in the previous technology is more, in order to reduce the number of gates; I have taken this project, to make high-throughput and low-cost effective.

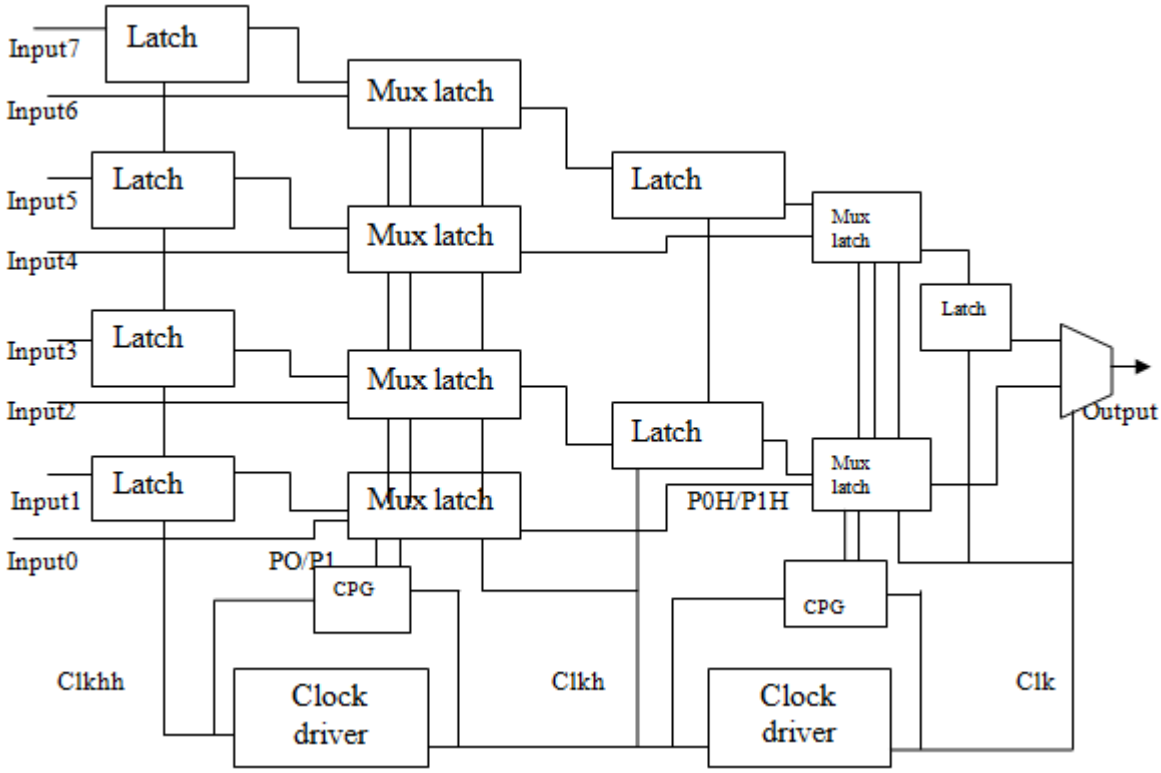

Fig.1.1 Transmission architecture with MUX-FFs

However this should help for serial link transmitters. To make**,** A Novel Low Gate-Count Pipeline Topology with Multiplexer-Flip-Flops for Serial Link, I am using a CML latches, CML MUX-FFs and clock pulse generator for reducing the gate-count in terms to reduce the area and power of the design. This design which help to increase the speed of transmission.

IV. EXPERIMENTAL RESULTS

In this project I am concluding that the number of gate count can be reduced by using MUX-FFs. And the power consumptions can be reduced. In this paper, a pipeline topology with MUX-FFs for serializer is proposed. The MUX-FF is composed of cascaded latches and MUX-Latches. Which is shown in below results complexity of circuit design is reduced in this architecture. The proposed 8-to-1 MUX-FFs help's to implement the 16-to-1 MUX-FFs and 32-to-1 MUX-FFs.These MUX-FFs can be implemented into two chips in the TSMC 90 nm and in 180 nm. Comparison between convention system and proposed system is shown below.

Table 1 Comparison with circuit diagram

Circuits	Conventional	Proposed
Latches	5(N-1)	N-1
MUX-Latches	-	N-1
Total	5(N-1)	2(N-1)

Fig. 1.2 comparison between convention system and proposed system

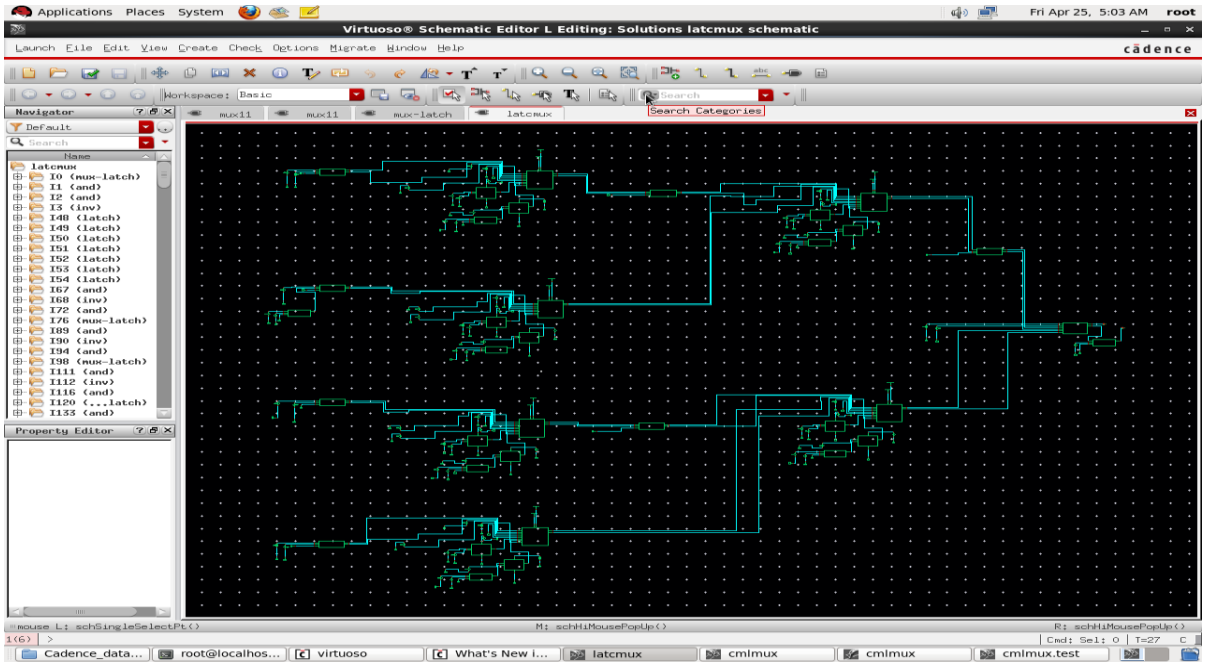

Fig.1.3. Serializer with MUX-FFs

Fig.1.4.Wave form for serilizer

V. CONCLUSIONS

In this paper, a pipeline topology with MUX-FFs for serializers is proposed. The MUX-FF is composed of cascaded latches and MUX-Latches. With the MUX-FFs, the gate-count number of the serializer has been

reduced by removing flip-flops from the conventional pipeline. And also power consumptions and area reduced about 63%.

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