

Review on Fault Tolerant Reversible Arithmetic N-bit Adder/ Subtractor

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Abstract: Programmable reversible logic circuit is design style for nanotechnology and quantum computing with minimum heat generation, quantum cost and garbage output. Late advances in reversible rationale utilizing and quantum PC calculations consider enhanced PC engineering and math rationale unit plans. In this paper, we survey the N-bit reversible logic adder and sub tractors are used with minimal delay, and may be configured to produce a variety of logical calculations. The reversible N-bit adder/ sub tractor design is verified and its advantages over the only existing adder design are quantitatively analyzed.

I. INTRODUCTION

This paper proposes an efficient fault tolerant reversible arithmetic logic unit. Traditional irreversible hardware computation inherently leads to the energy losses due to the missing bit information, where the energy dissipation is proportional to the number of missing bits [1]. Benet showed that to avoid this energy loss in a logic circuit is to use reversible logic gates [2]. A gate is reversible if there is a one-to-one mapping of the input/output. That is the relationship between input/output has to be an injective one. For this main reason, reversible logic has received significant attention and proven to have applications in areas such as optical computing, low power electronic design, DNA, quantum computing, and nanotechnology based systems to name a few [3],[4],[5]. It should be noted that the non-existence of both any fan out and feedback (loop) are two major problems with the reversible logic synthesis. Thus, the synthesis and implementation of the reversible logic circuit becomes more complex than the conventional one [4], [5] If a system is made up of fault tolerant components, then it will be able to continue operating properly when the failure occurs in some of its components. The discovery and revision of flaws in such blame tolerant frameworks are simpler. We can accomplish adaptation to internal failure in numerous frameworks by utilizing equality bits. Along these lines, equality protecting reversible circuit outline will be essential for improvement of issue tolerant reversible frameworks in nanotechnology which is a developing improved.

The advancement in VLSI designs, portable device technologies and increasingly high computation requirements, lead to the circuit design of faster, smaller and more complex electronic systems at the expense of lots of heat dissipation which would reduce the life of the circuit. Thus power consumption becomes an important issue in modern design. The power dissipation that is tolerable in a given application context is always limited by some practical consideration, such as a requirement that a limited supply of available energy (such as in a battery) not be used up within a given time, or by the limited rate of heat removal in one's cooling system, or by a limited operating budget available for buying energy. Thus, improving system performance generally requires increasing the average energy efficiency of useful operations. It has been unmistakably shown by Frank [7] that reversible figuring is the main feasible alternative to beat the force dispersal. The essential inspiration for reversible registering lies in the way that it gives the main way (that is, the main way that is sensibly steady with the most immovably settled standards of central material science) that execution on most applications inside practical force imperatives may at present keep expanding uncertainly. Reversible logic is also a core part of the quantum circuit model.

II. LITERATURE SURVEY

The examination on reversible rationale is being sought after towards both configuration and combination. In the amalgamation of reversible rationale circuits there have been a few fascinating endeavors in the writing, for example, the work in [2-3]. A reversible math rationale unit was planned by Thomsen, Gluck, and Axelsen [4] that depended on the V-formed outline of the Van Rentergem viper [5]. The ALU had five altered select lines, and delivered the accompanying consistent yields: ADD, SUB, NSUB, XOR and NOT. The least significant bit comprised of two Feynman gates and two Toffoli gates. Each additional bit also had two Fredkin gate.

M. D. Saiful Islam et al. [1], this article is concerned with the construction of a quantum-mechanical Hamiltonian describing a computer. This Hamiltonian produces a dynamical development which emulates an arrangement of basic coherent strides. This can be accomplished if each legitimate stride is locally reversible (worldwide reversibility is lacking). Computational blunders because of clamor can be remedied by method for

excess. Specifically, reversible mistake redressing codes can be inserted in the Hamiltonian itself. An estimate is given for the minimum amount of entropy which must be dissipated at a given noise level and tolerated error rate.

M. K. Thomsen et al. [2] “review on Reversible common sense Gates and their Implementation”, on this paper the Reversible common sense is one of the maximum crucial issue at gift time and it has unique areas for its utility, the ones are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, virtual sign processing (DSP), quantum dot mobile automata, conversation, laptop photographs. It is impractical to acknowledge quantum processing without usage of reversible rationale. The fundamental motivations behind outlining reversible rationale are to abatement quantum cost, profundity of the circuits and the quantity of trash yields. This paper gives the fundamental reversible rationale doors, which in outlining of more intricate framework having reversible circuits as a primitive part and which can execute more confounded operations utilizing quantum PCs. The reversible circuits shape the essential building piece of quantum PCs as all quantum operations are reversible. This paper presents the information identifying with the primitive reversible entryways which are accessible in writing and aides scrutinizes in outlining higher complex figuring circuits utilizing reversible doors.

Krishna Murthy et al.[5], “Design of a novel reversible ALU using an enhanced carry look- ahead adder” reversible rationale is increasing critical thought as the potential rationale outline style for usage in advanced nanotechnology and quantum registering with negligible effect on physical entropy. Late advances in reversible rationale permit plans for PC structures utilizing enhanced quantum PC calculations. Critical commitments have been made in the writing towards the configuration of reversible rationale door structures and math units, be that as it may, there are relatively few endeavors coordinated towards the outline of reversible ALUs. In this work, a novel programmable reversible rationale entryway is introduced and checked, and its usage in the outline of a reversible Arithmetic Logic Unit is illustrated. At that point, reversible executions of swell convey, convey select and Kogge-Stone convey look-ahead adders are dissected and thought about. Next, executions of the Kogge-Stone snake with sparsity-4, 8 and 16 were composed, checked and looked at. The upgraded sparsity-4 Kogge-Stone snake with swell convey adders was chosen as the best outline, and its executed in the configuration of a 32-bit math rationale unit is illustrated.

Jayashree H V et al.[4] “layout of green Reversible Binary Subtractors based on a new Reversible Gate”, this paper tells approximately the tremendous applications of Reversible common sense in quantum computing, low electricity VLSI design, quantum dot mobile automata and optical computing. While a few scientists have examined the configuration of reversible rationale components, there is very little work provided details regarding reversible paired subtractors. In this paper, we propose the outline of another reversible entryway called TR door.

III. REVERSIBLE GATE

Reversible rationale is picking up significance in zones of CMOS configuration on account of its low power dissemination. The customary entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Thus, one piece is lost every time a calculation is completed Hence it is impractical to decide a remarkable information that brought about the yield zero. With a specific end goal to make an entryway reversible extra information and yield lines are added so that a coordinated mapping exists between the info and yield. This keeps the loss of data that is fundamental driver of force dispersal in irreversible circuits. The information that is added to a $m \times n$ capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit. Those yields that are not utilized as a part of the circuit is called as junk yield (GO). The quantity of trash yield for a specific reversible door is not altered.

The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ **Basic Reversible Gates**

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

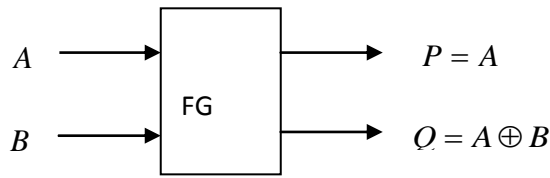


Figure 1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

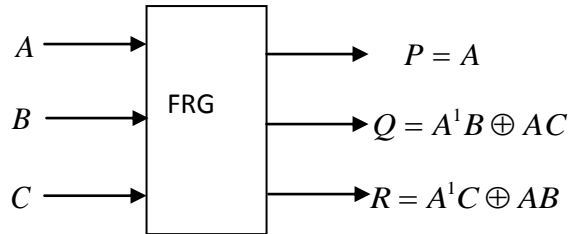


Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

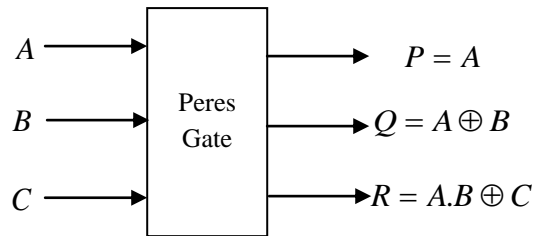


Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

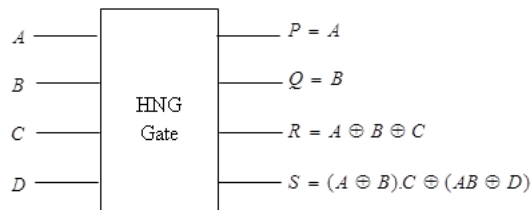


Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$\begin{aligned}
 P &= A & (5) \\
 Q &= A \oplus B & (6) \\
 R &= AB \oplus C & (7) \\
 S &= (AB \oplus C).C \oplus ((A \oplus B) \oplus D) & (8)
 \end{aligned}$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

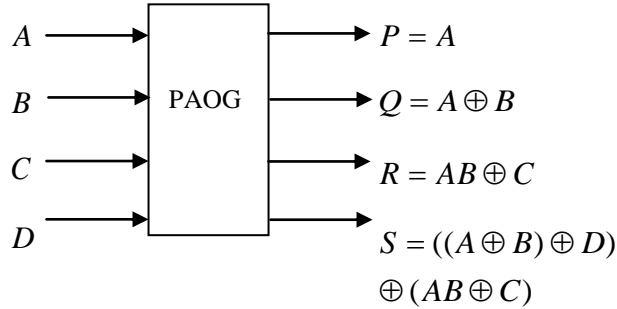
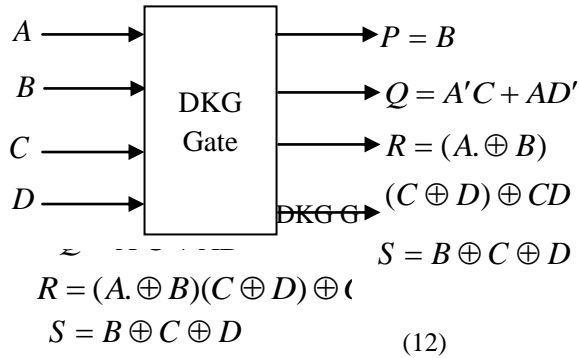


Figure 5: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:



IV. PROPOSED DESIGN

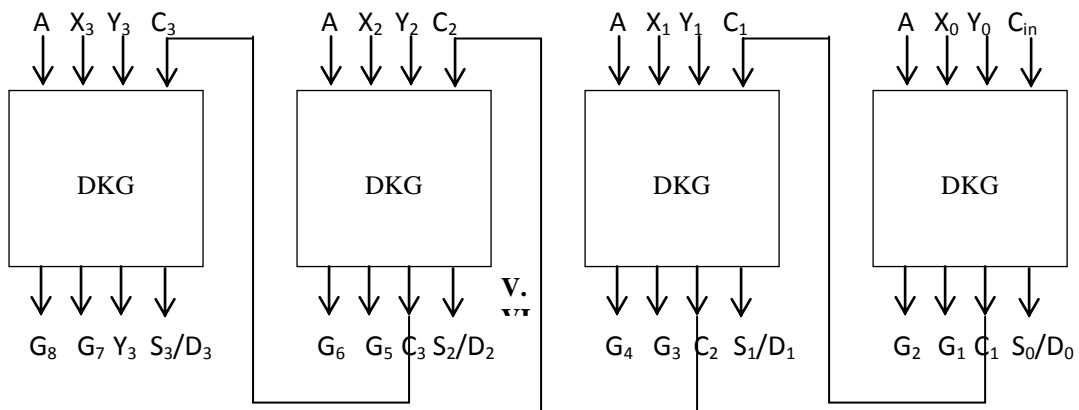
The N-bit Adder/ Sub tractor utilizes the DKG gate and DKG gate to produce two logical calculations: Adder and Sub tractor. The cost and delay calculations are identical to the 4-bit adder/ sub tractor in Figure 7. The proposed ALU is logical results based on the input opcodes are presented in Table 1.

Table 1: Reversible 4-bit Adder/ Sub tractor Opcodes and Logical Result for Proposed Design

A	X ₀	Y ₀	C _{in}	G ₂	G ₁	C ₁	S ₀ / D ₀
0	0	0	0	0	0	0	1/-
0	0	0	1	0	1	0	-/0
0	0	1	0	0	0	1	0/-
0	0	1	1	0	1	1	1/-
0	1	0	0	1	0	0	-/1
0	1	0	1	0	0	0	1/-
0	1	1	0	1	0	1	-/1
0	1	1	1	1	0	1	0/-

1	0	0	0	1	1	1	-/1
1	0	0	1	0	1	0	0/-
1	0	1	0	0	1	0	-/1
1	0	1	1	1	1	0	1/-
1	1	0	0	1	0	1	-/1
1	1	0	1	0	0	1	0/-
1	1	1	0	1	1	0	-/1
1	1	1	1	1	1	0	0/-

The binary full adder/sub tractor handles each input along with a carry in /borrow in that is generated as carry out/borrow out from the addition of previous lower order bits. If two n bit binary numbers are to be added or subtracted then n binary full adder/sub tractors should be cascaded. A parallel adder/sub tractor is the interconnection of a number of full adder/sub tractors and applying the inputs simultaneously. In this paper a 4 bit parallel adder/sub tractor circuit is designed using a 4x4 reversible DKG gate.



VII. SIMULATION RESULT

Table 2 shows the synthesis result for 4-32 bit. All the design verified the Xilinx 14.1 ISE simulator and different types of device family. Figure 2 shows the output of 4 bit reversible adder/sub tractor. The inputs to this module are the 4bit data „A“, „B“ and a control signal „A/S“. When the control input is 0“, the addition operation is performed and when the control input is 1“ subtraction operation is carried out. “Cin” indicates the carry in, Cout indicates the carry out or borrow out obtained from the circuit.

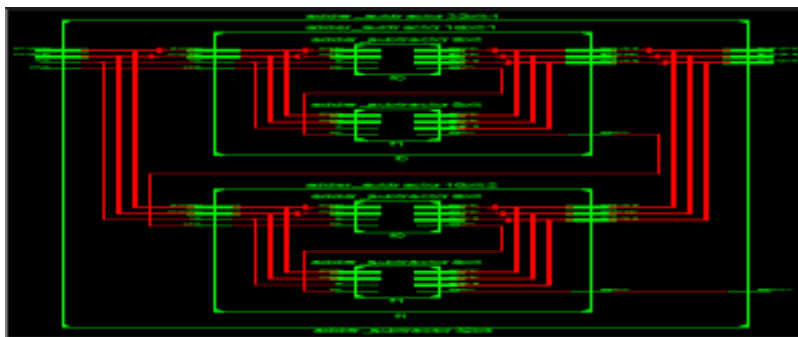


Figure 3: RTL view of 32-bit Adder/Sub tractor

Table 2: Syntheses Result for Reversible 4-bit, 8-bit, 16-bit and 32-bit Adder/Sub tractor with different Device Family

Device Family	Adder/ Subtractor	Number of Slice	4 Input LUTs	Maximum Combination Path Delay
Sparten 3	4-bit	6	11	9.498ns
	8-bit	12	22	11.236 ns
	16-bit	25	44	15.178 ns
	32-bit	49	88	22.266 ns
Sparten 3E	4bit	6	11	7.267 ns
	8-bit	12	22	8.798 ns
	16-bit	25	44	12.047 ns
	32-bit	49	88	18.109 ns
Sparten 6	4-bit	6	11	5.684 ns
	8-bit	12	22	7.011ns
	16-bit	25	44	8.502 ns
	32-bit	49	88	11.834 ns

VIII. EXPECTED OUTCOME

There previous algorithm reversible full adder/subtractor gate but, with the control bit it acts as either full adder or full subtractor. But in proposed design is given the result in simultaneous addition and subtraction. This gate gives sum and carry of three bits, as well as difference and barrow of those same three bits. Now we understand that this gate simultaneously acts as both full adder and full subtractor That means it obeys logical reversibility. In RACSG gate First output gives sum (or) difference output of full adder (or) full subtractor respectively, Second output gives the barrow output in full subtractor, Third output gives carry in full adder, Fourth output gives second input bit . Consider Fourth output as garbage output in adder and subtractor.

IX. CONCLUSION

The 4bit, 8bit, 16bit and 32bit Adder/ Sub tractor is designed by integrating various sub modules that includes DKG logic Gate. The performance assessment of the diverse sub modules are executed the usage of Xilinx 14.1 ISE Simulator and it was located that the circuits designed the usage of reversible common sense confirmed a reduced put off and power. As a future paintings more arithmetic and logical function may be used.

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