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Low Power Implementation of Mb-OFDMPHYModem for Wireless Sensor Network

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Abstract:- WSN demands low power and high speed data rate over network topology, Multi Band OFDM Physical Layer restricts the data rate and also consumes more power. The research work focuses on design and development of low power high speed PHY layer for WSN based on MB-OFDM standards. The paper primarily involves design and implementation of MB- OFDM UWB physical layer for high data rate based on Wavelets for WSN on hardware platform. The modified lifting wavelet transform are used for designing wavelets and performing the transform, it is able to increase the spectral efficiency and also decrease the bit error rate compare to FFT/IFFT based OFDM. The convolution-based 1-dimentional DWT requires both arithmetic computations and a large memory for storage. Such features are not suitable for high speed or low-power applications. Convolutional encoding with Viterbi decoding is a powerful method for forward error detection and correction. The Viterbi decoder uses full-parallel structure to improve computational speed and to avoid overflow of the data. Compared to the generic Viterbi decoder, this design can effectively decrease the 10% of chip logic elements, reduce 5% of power consumption and increase the encoder-decoder working performance in the hardware implementation.

Keywords:- WSN, MB-OFDM, Viterbi decoder, Convolution encoder, DWT/IDWT

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation scheme that transmit data over number of orthogonal subcarrier .In FDM (frequency division multiplexing) there is no relationship between the carrier frequencies like f1,f2,f3 but in OFDM there must be strict relation between frequency of sub carrier.

$$fn = f1 + n\nabla f \quad (1)$$

$$\backslash where\ \nabla f = (1/Tu) \quad (2)$$

In single carrier system if signal get fade or interfered then entire link gets failed where as in multicarrier system only a small percentage of the subcarriers will be affected. Where FFT based OFDM has ISI and large bandwidth occupancy which cannot satisfy the future needs. This project proposes implementation of new modified lifting wavelet transform for designing wavelets and performing the transform. By implementing LDWT, it is able to increase the spectral efficiency andalso reduce the bit error rate. A basic OFDM system consists of a QAM or PSK modulator/demodulator, a serial to parallel/ parallel to serial converter, and an IFFT/FFT or DWT/IDWT module. Using FPGA instead of an ASIC gives flexibility for reconfiguration.

The next section of this paper is organized as follows: section-2 Architectural design of DWT/IDWT; section-3 Architectural design of Convolutional encoder and Viterbi de- coder; section-4 Implementation of DWT/IDWT; section-5 Implementation of Convolutional encoder and Viterbi decoder; section-6 simulation results of proposed system; section 7 gives conclusion and future work.

A. Proposed system

The figure 1 gives data flow diagram of proposed system.

Fig. 1. Data Flow diagram of MB-OFDM

Suppose this transmission takes four seconds. Then, each piece of data in the left picture has duration of one second. On the other hand, OFDM would send the four pieces simultaneously as shown on the fig1 right. In this case, each piece of data has time 4 seconds. This large duration leads to fewer problems with inter carrier interference. One more rea- son to consider OFDM is low-complexity implementation for high-speed systems compared to single carrier techniques.The OFDM system have the following advantages:(i) by allowing overlap of carriers it uses the spectrum; (ii) by dividing the channel into narrow band flat fading sub channels, OFDM is more resistant to frequency selective fading than the single carrier system; (iii) eliminates ISI and ICI with the use of guard band extension cyclic prefix. Though the OFDM has advantages, They are indicated as follows: (i) the OFDM signalhas a high Peak to Average Power Ratio due to overlapping of subcarriers; (ii) multipath propagation must be neglected so that orthogonally will not be affected, and (iii) phase noise and Image Rejection are also a problem in OFDM.ICI means that the orthogonal between different sub channels in the OFDM signals is destroyed there are two causes of ICI i) delay spread of radio channel ii) exceeds guard interval.

B. Reviews of related research

The low power MB-OFDM architecture implemented on have reduced the gate count by 28% with power dissipation less than 381mW operating at 66MHz for WSN frequency of operation should be around 200Mw and should consume power less than few mW DSTFC Codes have successfully used for MB-OFDM UWB, however DSTFC for WIMAX MIMO still not been explored. MB-OFDM UWB Receiver has been implemented on FPGA and ASIC platform, the simulation results on hardware implementation does not match with MATLAB simulation results due to quantization noise, there is a need for optimized hardware architecture for MB- OFDM UWB. FFT/IFFT processors are been adopted for orthogonal modulation, FFT/IFFT introduce complexity and hence delay. In order to improve performance of MB-OFDM UWB wavelets could be used to replace FFTs for large set of data streams such as Giga bits transmission memory scheduling schemes could be adopted, very few literature report memory scheduling scheme with 100% utilization.

II. ARCHITECTURAL DESIGN OF DWT/IDWT The DWT CAN BE LOOKED AT AS THE MULTI RESOLUTION DECOM-

The DWT can be looked at as the multi resolution decomposition of a sequence. It takesa length N sequence z (n) as input and generates a length N sequence as the output. The output can be viewed as the multi resolution representation of z(n), and has N/2 values at the highest resolution and N/4 values at the next resolution and so on. That is the frequency resolution is low at the high frequencies and high at the low frequencies, while the time resolution is high at the higher frequencies and low at the lower frequencies.

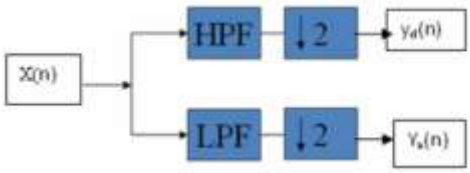

Fig. 2. Block Diagram of DWT

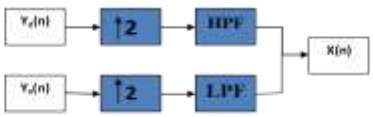

Fig. 3. Block Diagram of IDWT

The IDWT can be looked at as the multi resolution de- composition of a sequence. It takes a Ya(n),Yb(n) as input and that input samples up sampled by 2 then convolution with HPF and LPF generates a sequence as the output. The output can be viewed as the multi resolution representation of x(n).

A. Modified Lifting DWT

The lifting coefficients were substituted and the results were scaled by multiplying with 256 to avoid decimal and to round off the values. The lifting scheme found that the final scaling and dilation coefficients are interdependent on predict and update outputs, thus there is s a delay and also affects throughput. To reduce delay and improve the throughput of DWT computation it is required to minimize the inter dependence in partial outputs of lifting scheme is modified lifting scheme is derived. The modified lifting scheme equations

are realized using multipliers, adders and intermediate register. Shift adder is chosen for faster operation. Carry save adder is adopted for addition operation as it uses minimum gates and also has very small delay compared with ripple carry adder. The input samples are stored into the input data register, after every 9 clock cycles the multiplication and addition operations are performed. Computation of ai and di coefficients requires 4 clock cycles. Fig 5 Thus the latency of the proposed architecture is 13 clock cycles (9 + 4), and the throughput is 5 clock cycles. Fig 6 the modified lifting based DWT architecture is faster than generic DWT architecture by 4 clock cycles. The Figure 4 below gives the block diagram of modified Lifting DWT

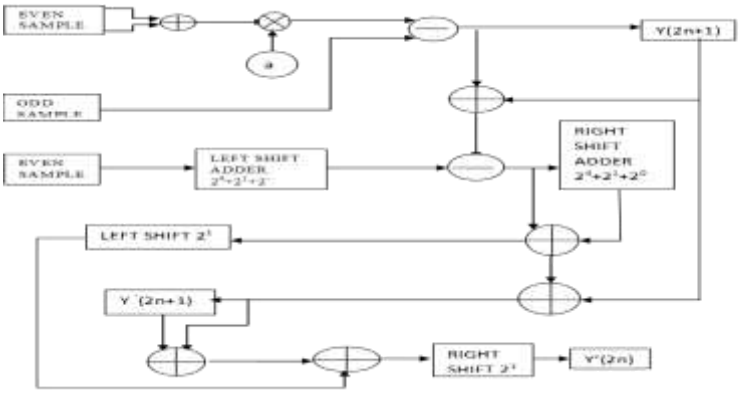

Fig. 4. Modified DWT

The modified lifting scheme equation is as follows

i) **Split step**

Even Samples Xe← $X(2n)$ (3)

Odd Samples Xo ← $X(2n + 1)$ (4)

ii) **lifting step**

$Y(2n + 1) = X(2n + 1) + a(X(2n) + X(2n + 1))$ (5)

A is greater than one so same equation as LDWT/DWT Modified equation

$Y(2n) * (1/b) = X(2n) * (1/b) + (Y(2n-1) + Y(2n+1))$ (6)

Where b=1/0.0529=18.92=19 i.e 19=16+2+1=24+21+20

Y(2n) * (1/b) = X(2n)*(1/b) + (Y(2n-1) + Y(2n+1))

Previous equation we are using addition after multiplication so it takes delay so to reduce delay we are using shifting

Y(2n+1)*(1/c) = Y(2n+1)*(1/c) + (Y(2n) + Y(2n+2)) Where c=(1/0.8829)=0.923=1

$Y(2n + 1) = Y(2n + 1) + (Y(2n) + Y(2n + 2))$ (7)

Y(2n) *(1/d)= Y(2n)*(1/d) + (Y(2n-1) + Y(2n+1)) Where d=1/0.4435=1.92=2=21

$Y(2n) * (21) = Y(2n) * (21) + (Y(2n - 1) + Y(2n + 1))$ (8)

iii) **Scaling step**

$Y(2n + 1) = -kY(2n + 1)$ (9)

$Y(2n) = Y(2n)/k$ (10)

These modified algorithms of forward transform output given to inverse transform of modified algorithms.

B. Modified Lifting IDWT

The figure below gives the modified lifting IDWT block diagram

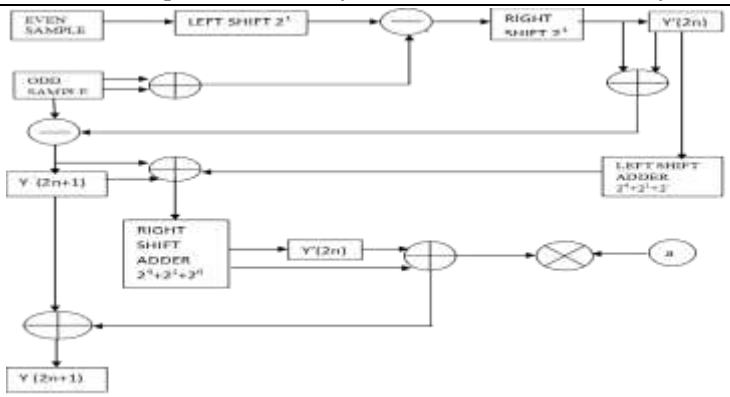

Fig. 5. Modified Lifting IDWT

i) **Scaling step**

$X(2n) = kY(2n)$ (11)

$X(2n + 1) = (-Y(2n + 1))/k$ (12)

Modified algorithms of inverse transform inputs from for- ward transform of modified algorithms this outputs given to lifting step then combine step to get back original signal

ii) **Lifting step**

$X(2n) * (21) = X(2n) * (21) - d(X(2n-1)+X(2n+1))$ (13)

$X(2n + 1) = X(2n + 1) - (X(2n) + X(2n + 2))$ (14)

$X(2n) * (24+21+20) = X(2n) * (24+21+20) - (X(2n-1)+X(2n+1))$ (15)

$X(2n + 1) = X(2n + 1) - a(X(2n) + X(2n + 2))$ (16)

iii) **Combine step**

Even Samples $Xe \leftarrow X(2n)$ (17)

Odd Samples $Xo \leftarrow X(2n + 1)$ (18)

III. ARCHITECTURAL DESIGN OF CONVULUTIONAL ENCODER AND VITERBIDECODER

A. Convolutional Encoder

The Convolutional encoder is a strong encoding technic. Convolutional code is a type of error-correcting code in which each (n:m) m-bit information symbol (each m bit string) to be encoded is transformed into an n-bit symbol, where m/n is the code rate (n:m) and the transformation is a function of the last k information symbols, where K is the constraint length of the code. Figure 6 shows the convolutional encoder of constraint length 7 with 3 output template is designed so that author affiliations are not repeated each time for multiple authors of the same affiliation.

The encoder equations are as shown

$g(0) = data\ in \oplus_q (1) \oplus_q (2) \oplus_q (4) \oplus_q (5)$ (19)

$g(1) = data\ in \oplus_q (0) \oplus_q (1) \oplus_q (3) \oplus_q (5)$ (20)

$g(2) = data\ in \oplus_q (0) \oplus_q (1) \oplus_q (2) \oplus_q (5)$ (21)

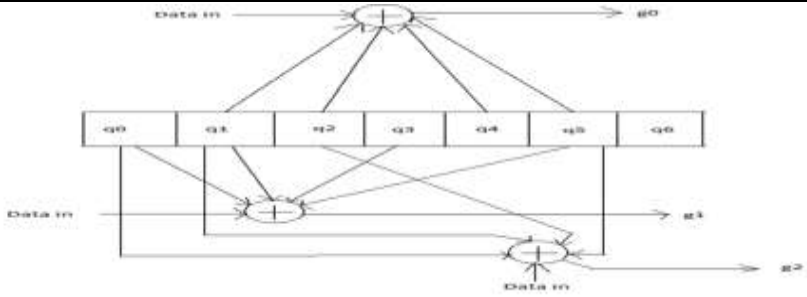

Fig. 6. The rate 1/3 Convolutional Encoder

Let the input bit be 1 that is Data in =1

Step1:-0000001

The corresponding 7 values which has been taken by q with respect to figure 6 are as shown.

q6=0, q5=0, q4=0, q3=0, q2=0, q1=0, q0=1;

$$g(0) = \oplus 1 \oplus 0 \oplus 0 \oplus 0 \oplus 0 = 1$$
$$g(1) = \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$$
$$g(2) = \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$$

g=001

Step2:-0000011

q6=0, q5=0, q4=0, q3=0, q2=0, q1=1, q0=1;

$$g(0) = \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$$
$$g(1) = \oplus 1 \oplus 1 \oplus 1 \oplus 0 \oplus 0 = 1$$
$$g(2) = \oplus 1 \oplus 1 \oplus 1 \oplus 0 \oplus 0 = 1$$

g=110

Step3:-0000111

q6=0, q5=0, q4=0, q3=0, q2=1, q1=1, q0=1;

$$g(0) = \oplus 1 \oplus 1 \oplus 1 \oplus 0 \oplus 0 = 1$$
$$g(1) = \oplus 1 \oplus 1 \oplus 1 \oplus 0 \oplus 0 = 1$$
$$g(2) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$

g=011

Step4:-0001111

q6=0, q5=0, q4=0, q3=1, q2=1, q1=1, q0=1;

$$g(0) = \oplus 1 \oplus 1 \oplus 1 \oplus 0 \oplus 0 = 1$$
$$g(1) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$g(2) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$

g=001

Step5:-0011111

q6=0, q5=0, q4=1, q3=1, q2=1, q1=1, q0=1;

$$g(0) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$g(1) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$g(2) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$

g=000

Step6:-0111111

q6=0, q5=1, q4=1, q3=1, q2=1, q1=1, q0=1;

$$g(0) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 1$$
$$g(1) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 1$$
$$g(2) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 1$$

g=111

Step7:-1111111

q6=1, q5=1, q4=1, q3=1, q2=1, q1=1, q0=1;

$g(0) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 1$

$g(1) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 1$

$g(2) = \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 1$

g=111

B. Viterbi Decoder

The principle of Viterbi algorithm is maximum likelihood decoding however, it reduces the computational load by taking advantage of the special structure in the code trellis. The advantage of Viterbi decoding compare with brute-force de- coding is that the complexity of a Viterbi decoder is not a function of the number of symbols in the code word sequence The algorithm involves calculating a measure of similarity, or distance, received signal, at time ti and all the trellis path entering each time at ti. .When two paths entering the same state, the one having the best metric is chosen; this path is called the surviving path. This selection of surviving paths is performed for all the states the decoder continues in this way to advance deeper into the trellis, making decisions by eliminating the least likely path .The early rejection of un likely paths reduces the complexity. Note that the goal of selecting the optimum path can be expressed, equivalently, as choosing the code word with the maximum likelihood metric, or as choosing the code word with the minimum distance metric. Viterbi decoding was first shown to be an efficient and practical decoding technique for short constraint length codes by Heller. Forney and Omura demonstrated that the algorithm was in fact maximum. It uses trellis diagram to compute branch metric and path metric from received signal to possible transmitted signal.

The general structure of Viterbi decoder is as shown in figure 7 below

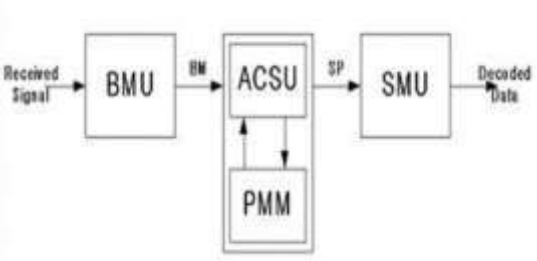

Fig. 7. The General Structure of Viterbi Decoder

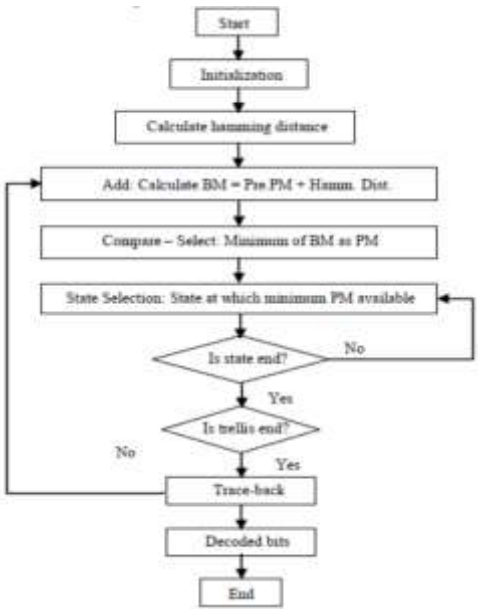

Fig. 8. Design flow graph of Viterbi Decoder

IV. IMPLEMENTATION OF DWT/IDWT

In digital circuit design, RTL (Register-Transfer Level) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers and the logical operations performed on those signals. RTL abstraction is used in HDL to create high level representations of a circuit from which lower level representations and ultimately actual wiring can be derived.

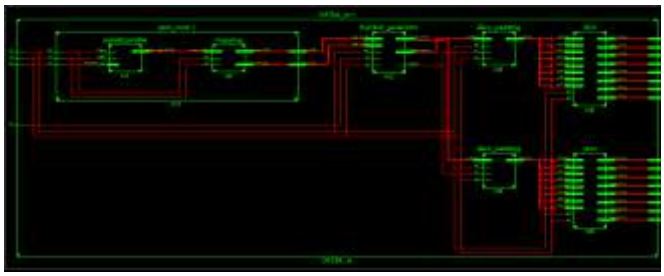

Fig. 9. Internal structure of OFDM DWT/IDWT Transmitter

The Figure 10 shows the internal architecture as viewed in the RTL schematic window of OFDM receiver consistsDWT, inverse zero padding, inverse symbol generator, QAM demodulation. After OFDM transmitter output is given to OFDM receiver to get back original signal.

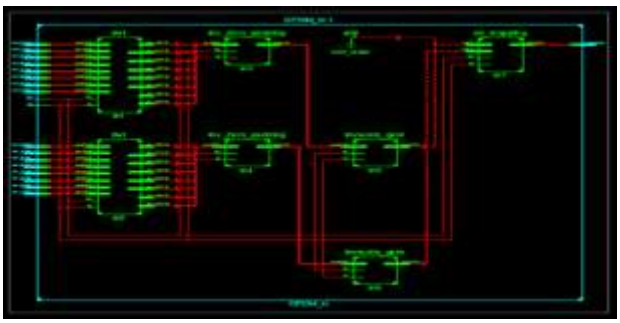

Fig. 10. Internal Architecture of OFDM DWT/IDWT receiver

V. IMPLEMENTATION OF CONVOLUTIONAL ENCODER AND VITERBI DECODER

The RTL schematic of convolutional encoder is as shown in figure 11 .It takes the1 bit input value and generates the 3 bit output value. The convolution process is done only when reset is 0 and enable is 1.

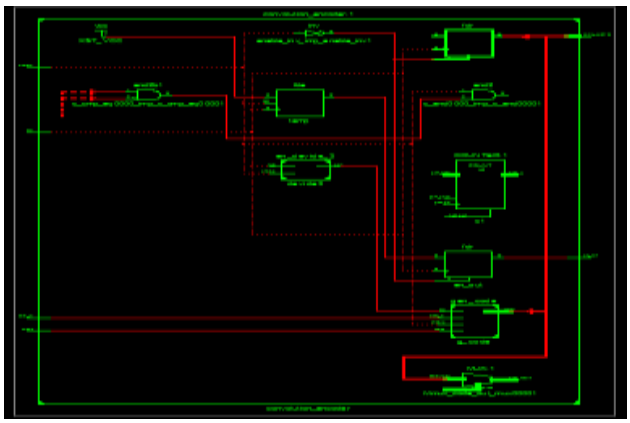

Fig. 11. Internal Structure of convolutional Encoder

The RTL schematic of Viterbi decoder is as shown in figure12. It is a combination of BMU; ACS and SMU .It takes convolutional encoded bit as inputs and gives back the original bit which is transmitted.

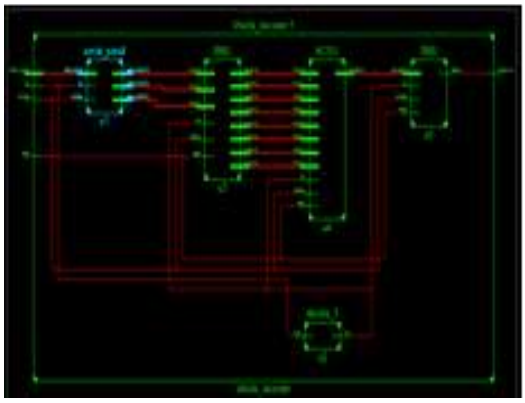

Fig. 12. Internal Structure of Viterbi Decoder

SIMULATION RESULTS

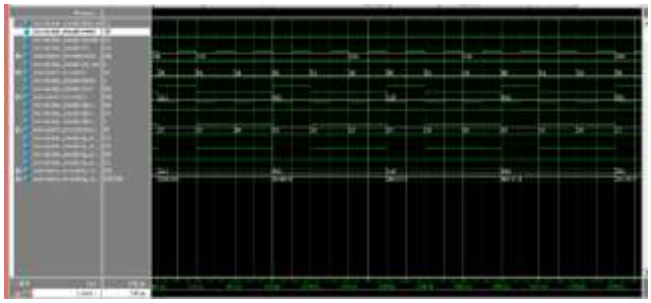

Fig. 13. Simulation results of convolutional encoder

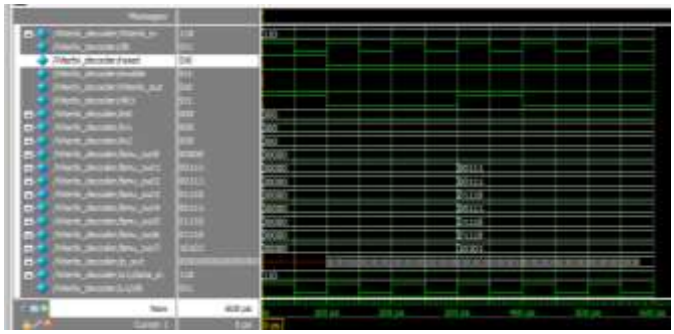

Fig. 14. Simulation results of Viterbi Decoder

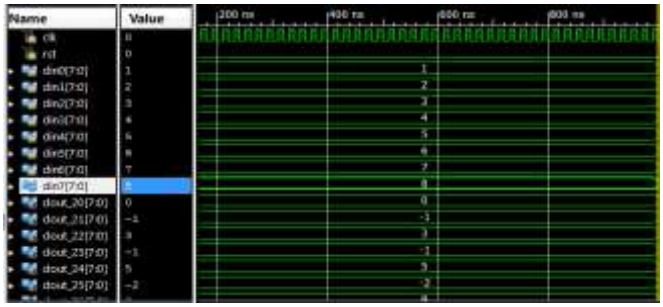

Fig. 15. Simulation results of DWT

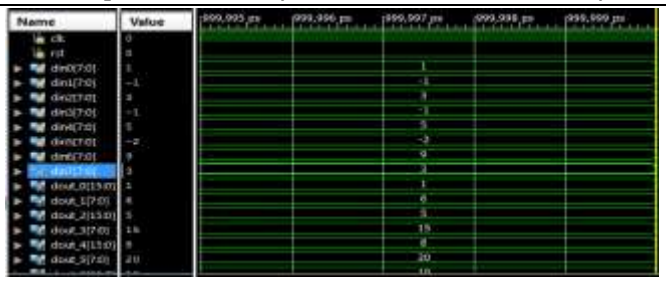

Fig. 16. Simulation results of IDWT

VI. CONCLUSION

It is well-known that, for systems that deploy conventional convolution codes, a Viterbi decoder is the best solution in maximum likelihood sense to decode an information sequence. Viterbi decoder uses Euclidean or Hamming distance as ametric. The research work presented an Convolution encoder and Viterbi decoder for constraint length 7 and bit rate 1/3 is implemented using Verilog HDL and simulated using ModelSim. The research work explains step by step working of three basic modules (BMU, PMU and SMU) of Viterbi decoder and it gives the simulation result of each module. we have obtained advantageous results in terms of speed, high data rate. The paper proposes implementation of new modified lifting wavelet transform for designing wavelets and performing the transform. By implementing LDWT, it is able to increase the spectral efficiency and also decrease the bit error rate.DWT based OFDM is finding importance due to its performance in terms of ISI and bandwidth compatibility over FFT based OFDM. The DWT-OFDM outperformed FFT-OFDM in BER, Haar wavelet showed best performance over Biorthogonal (bior3.3, bior5.5), Daubechies (db2,db4), reverse biorthogonal (rbior3.3, rbior5.5) by approximately 2dB. However, computation complexity of DWT restricts use of DWT for OFDM due to its hardware requirements on VLSI platform. In this work, lifting based DWT is modified and a new architecture is derived that can compute DWT in less, and consumes powerless.

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