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Design and Analysis of Fractional Order Transistor Amplifier.

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ABSRACT
The aim of this paper is to compare the performance of fractional order RC based transistor amplifier with its fractional counterpart. Here, the fractional order capacitor is being designed in domino logic in passive symmetric realization both in simulation and experimental level and the phase angle evaluated is being compared with the actual order. The fractional capacitor is being designed by calculating certain equations and determining the values of resistances and capacitances for required order of the fractional capacitor. The fractional order capacitor designed in MATLAB Simulink is implemented in BJT based RC coupled amplifier and the frequency domain analysis is obtained and compared with the orders of fractional capacitor (α=0.6, 0.8 and 1.0). The order of α providing the maximum bandwidth resulting in minimum selectivity is being observed.

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I. INTRODUCTION

Analog amplifiers are used to amplify analog signal. Here three capacitors are used as reported in [1]. Analog amplifier circuit used three capacitors named as C_c, C_{in}, C_E, C_C and C_{in} determines the bandwidth response of the amplifier. C_E are used for biasing purpose. In this paper three capacitors are replaced three fractional capacitors which based on fractional calculus. Fractional calculus is a branch of mathematical studies. Fractional calculus defined as extension of derivative and integrals to non-integer order. It studies the possibility of taking real number or even complex number. The power of the differential operator and integer operator is "j". The fractional order circuits can be finding practical use in dynamic system in biology, physics, viscoelasticity and electrochemistry. Also, fraction-order system can be used in electrical engineering, telecommunication and agriculture. Fractional-order equivalent circuit models are a simple and effective method of representing experimental measurements of the electrical impedance and phase of fractional order elements. Using this method requires knowledge of the fractional-order models appropriate for the specific application and understanding how to apply optimization procedures to fit models to experimental datasets. This chapter has introduced recent progress and applications of fractional-order models, their underlying mathematics and circuit simulation and coding models.[2]

As the conventional calculus is very popular among science &or engineering community the fractional calculus is not so popular [3]. The fractional capacitor cannot be directly simulated so first replaced the fractional capacitor with a domino ladder circuit. Different methods for approximation of a fractional-order transfer function can be used [5-8].

II. THEORETICAL BACKGROUND OF FRACTIONAL CAPACITOR

Fractional capacitor is a passive circuit element it gives 0 to -90-degree phase angle and remains constant with frequency. The impendence of a fractional capacitor can be expressed as [9]

$$Z = \frac{1}{C_F S^{\alpha}} \tag{1}$$

Here C_F is the fractional capacitance of Fractional capacitor and α is the order of fractional capacitor. Also, α is known as Fractional operator. It is used to interpret the voltage – current relationship of a fractional capacitor [10].

The last two decades have seen considerable progress in research on fractional-order circuits and system. Fractional calculus was mostly restricted as a research topic among the mathematicians only [2, 3]. But several applications of fractional calculus came into light recently in electrochemistry [4], thermal processes [8, 9], diffusion-wave [10, 11], and analog circuits [12-14]. The behaviours of these systems were found to be better explained by fractional-order deferential equations rather than using classical integer order deferential equations [15]. Conventional capacitors and inductors are characterized by first order deferential equations. The unit of fractional capacitance is $F/s^{1-\alpha}$. Here 's' indicates time in second and 'F' indicates Farad. [16]

Here, in simulation a domino logic fractional capacitor is being designed for operation of similar to that of fractional capacitor. This capacitor is being constructed by cascading resistors and capacitors of desired values to obtain the respected fractional order.

III. PERFORMANCE ANALYSIS OF DOMINO LADDER CIRCUIT:

The fractional capacitor cannot be directly simulated so that first replaced the fractional capacitor with a domino ladder circuit. This section concise the Fractional capacitors simulated by different configurations of resistance and capacitance. There is huge amount of work found in literature where the simulation of fractional capacitance has been studied using ladder network e.g. cross resistance capacitance ladder, Domino ladder network, nested ladder. There are Different structured of domino ladder circuit (Figure.) which are obtainable in literature [18-20]. The domino ladder circuits are more acceptable in designing different values of α than cross ladder network. The domino ladder shown in Figure. has fascinated for simulation of fractional order circuit. In domino ladder network of Figure. values of the Resistance and Capacitance used are in geometric progression. The ratio of resistance being (g>1) and the ratio of capacitance being (G>1)[21].By assigning different values of g and G we can varied the order of Fractional Capacitance.
The domino ladder networks impendence can be expressed as

$$Z(s) = 1/C_F S^{\alpha} \quad (2)$$

Here,

$$\alpha = (1-\gamma) \quad (3)$$

$$\gamma = \frac{\ln (G)}{\ln (Gg)} \quad (4)$$

$$\frac{1}{C_F} = \frac{\pi cosec(\pi\gamma) R_0^{\gamma}}{\ln (Gg) C_0^{1-\gamma}} \quad (5)$$

$0 < \gamma < 1$

$$R_j = g^{-j} R_0 \quad (6)$$

$$C_j = G^{-j} C_0 \quad (7)$$

By using the above equations [22-25] here I have found the values for different resistors and capacitors for different fractional order (α). Here, the value of R_0=1KΩ and C_0=0.01F
By using equation (6) and (7) we found the value of resistors and capacitors:

Table.1 Resistance data reorientation at different fractional orders of α.

Parameters	α=0.8	α=0.6	α=0.4
R_0	1MΩ	1MΩ	1MΩ
R_1	0.48MΩ	0.76KΩ	0.89 MΩ
R_2	0.23MΩ	0.59KΩ	0.79 MΩ
R_3	0.11MΩ	0.45KΩ	0.71 MΩ
R_4	0.5KΩ	0.35KΩ	0.63 MΩ
R_5	0.2KΩ	0.26KΩ	0.56 MΩ
R_6	0.13KΩ	0.20KΩ	0.50 MΩ
R_7	0.06K	0.15KΩ	0.45 MΩ
R_8	0.03KΩ	0.12KΩ	0.40 MΩ

The values for capacitors are C_1=8.3mF, C_2=6.9mF, C_3=5.7mF, C_4=4.8mF, C_5=4mF, C_6=3.3mF, C_7=2.7mF, C_8=2.3mF

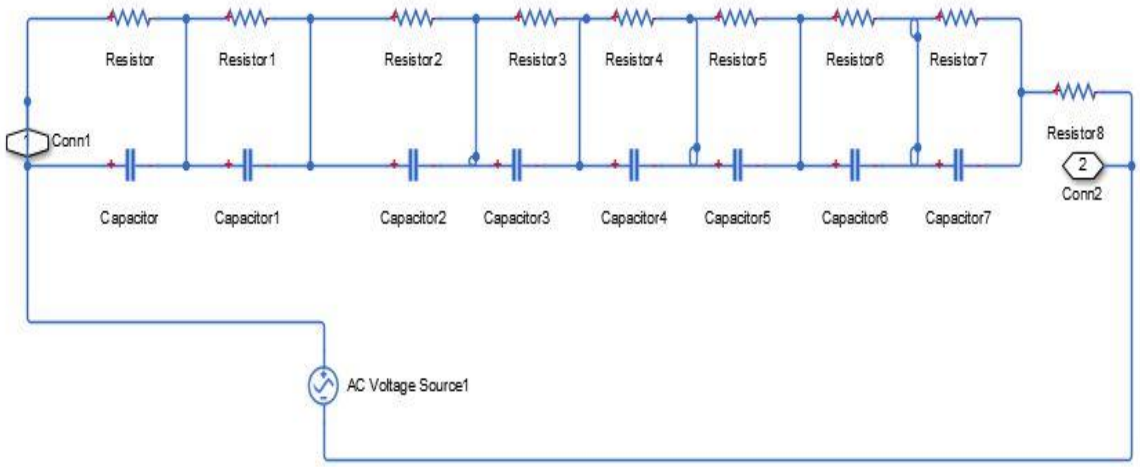
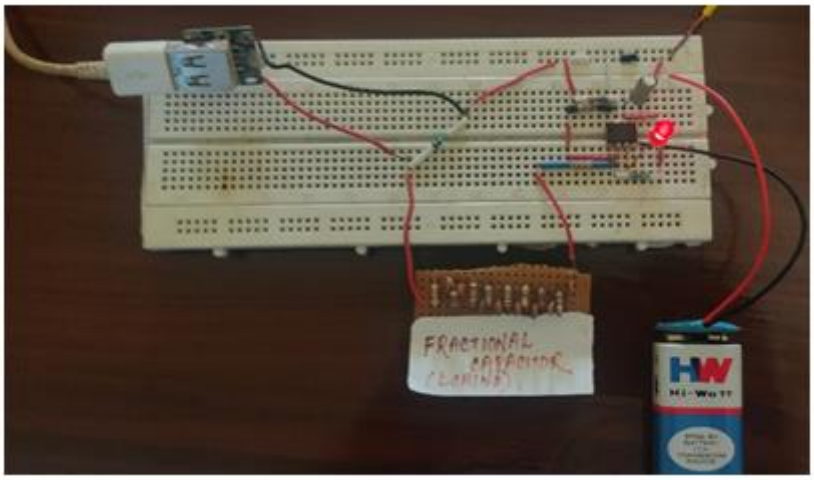
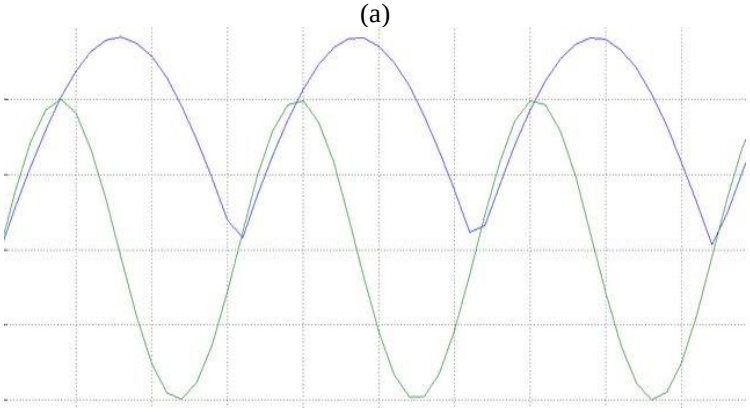


Figure.1 Domino ladder circuit in MATLAB R2016a.

In the simulation in MATLAB, Simulink, the domino ladder circuit is being implemented in passive symmetric network of a fractional order capacitor where the varying values of prescribed resistances and capacitances changes the order of the prescribed fractional order circuit effectively. In, experimentation the domino ladder circuit is being implemented using passive symmetric circuit as follows in Figure.



(a)



(b)

Figure.2 Experimental analysis of fractional order capacitor in domino logic operation.

In fig 2(a) a fractional passive symmetric circuit is being designed using the series of capacitors proving the 0.8th order of the fractional capacitor as seen in the table with the appropriate values of resistances and capacitances. In fig 2(b) the Zelscope (Digital Oscilloscope) Sine wave output to the fractional capacitor with a 1 Ω is being observed.

Where, we observed that we have a phase shift of -71.68° which is being analysed in fractional domain evaluates to,

$$C_1 \times \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \sin t \; d^{\alpha}t = -\alpha\frac{\pi}{2} = -71.68$$
$$\text{where, } \alpha = 0.796 \approx 0.8 \tag{8}$$

As the capacitor's control design performs the operation of a unit integrator, therefore integration is carried out of the sine wave which is provided as input to check the order of the fractional capacitor designed. In, equation 8 the fractional order of the capacitance is being calculated as obtained phase angle from the experiment.

IV. DOMINO LOGIC IMPLEMENTATION OF FRACTIONAL ORDER BJT BASED R-C COUPLED AMPLIFIER.

A Resistance Capacitance (RC) Coupled Amplifier is basically a multi-stage amplifier circuit extensively used in electronic circuits. Here the individual stages of the amplifier are connected together using a resistor–capacitor combination due to which it bears its name as RC Coupled. Here, the C_E is also called bypass capacitor which passes only AC while restricting DC, which causes only DC voltage to drop across R_E while the entire AC voltage will be coupled to the next stage. further, the coupling capacitor C_O also increases the stability of the network as it blocks the DC while offers a low resistance path to the AC signals, thereby preventing the DC bias conditions of one stage affecting the other. In addition, in this circuit, the voltage drop across the collector-emitter terminal is chosen to be 50% of the supply voltage V_{CC} in order to ensure appropriate biasing point.

This circuit is designed by using various resistors and capacitors in MATLAB Simulink

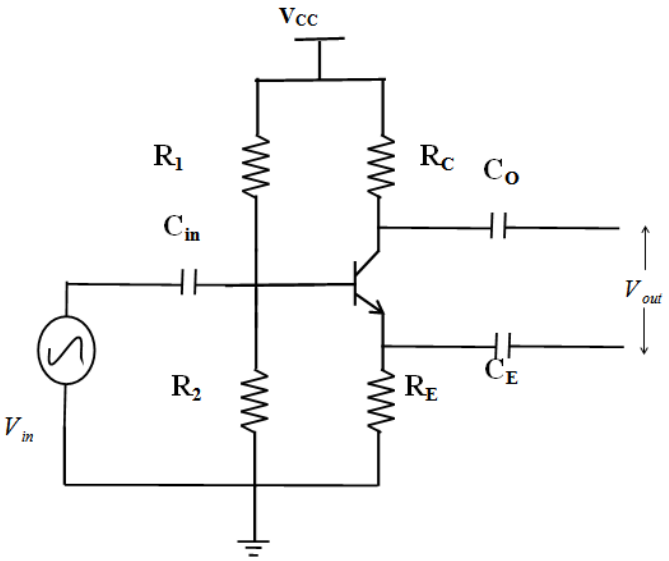


Figure.3. Circuit diagram of R-C Coupled amplifier.

In the above figure we represent a fractional BJT based amplifier circuit whose values are given in the table below

Table.2. Components description as used in simulation analysis.

R_1	R_2	R_L	R_E	C_{in}	C_E	C_{out}
39kΩ	4.7kΩ	3.9kΩ	1.2kΩ	1μF	1μF	1μF

From the circuit in Figure.2 the current equations are found to be

$$V_{CE} = V_{CC} - R_C I_C = V_{CC} - R_C \, I_S e^{\frac{V_{in}}{V_T}} \tag{9}$$
$$V_{CC} - R_1 I_1 - \frac{1}{C_{in} S} = V_{in} \tag{10}$$

$$V_{CC} - R_C I_C - \frac{1}{C_{out} S} = R_E I_E - \frac{1}{C_E S} = V_{out} \tag{11}$$

The above equation when implemented in fractional domain can be represented as,

$$V_{CC} - R_1 I_1 - \frac{1}{C_{in} S^{\alpha}} = V_{in} \tag{12}$$

$$V_{CC} - R_C I_C - \frac{1}{C_{out} S^{\alpha}} = R_E I_E - \frac{1}{C_E S} = V_{out} \tag{13}$$

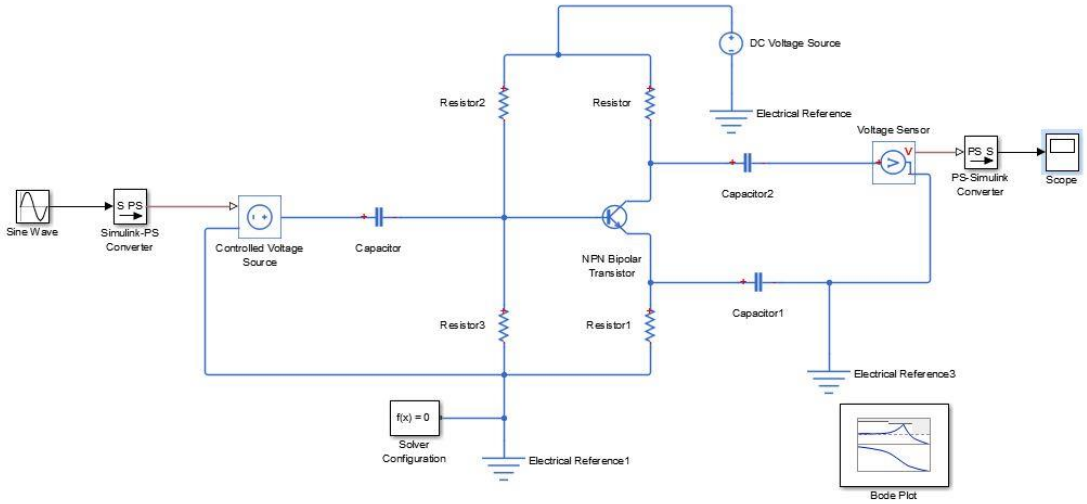


Figure.4. Simulink model of integer order rc based amplifier.

In, the Figure.3 the implementation of classical BJT based single stage amplifier is being designed and the frequency domain analysis is being carried out I MATLAB R2016a.

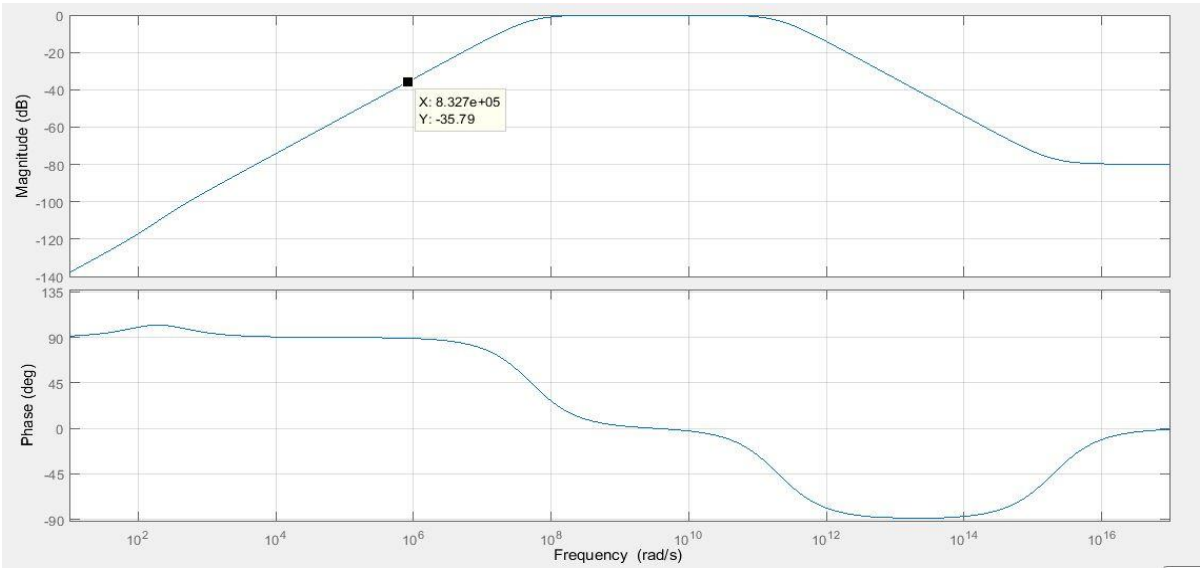
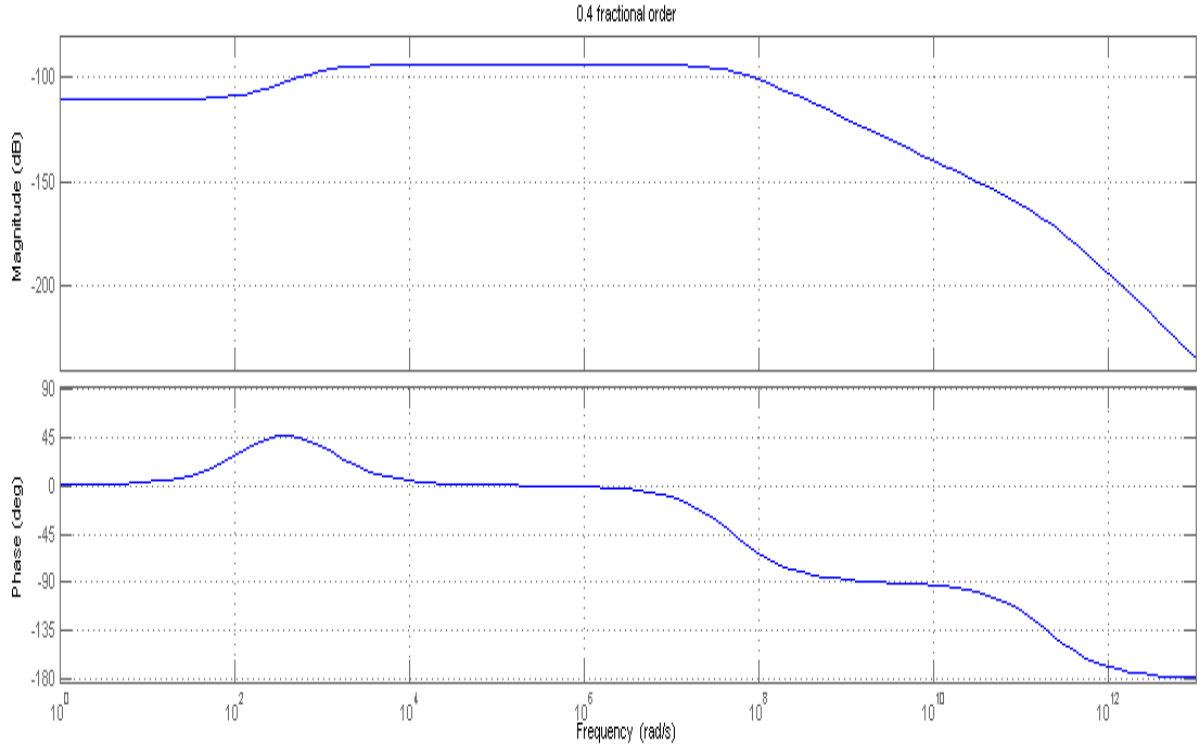


Figure.5 Magnitude and phase plot of the integer order rc based amplifier.

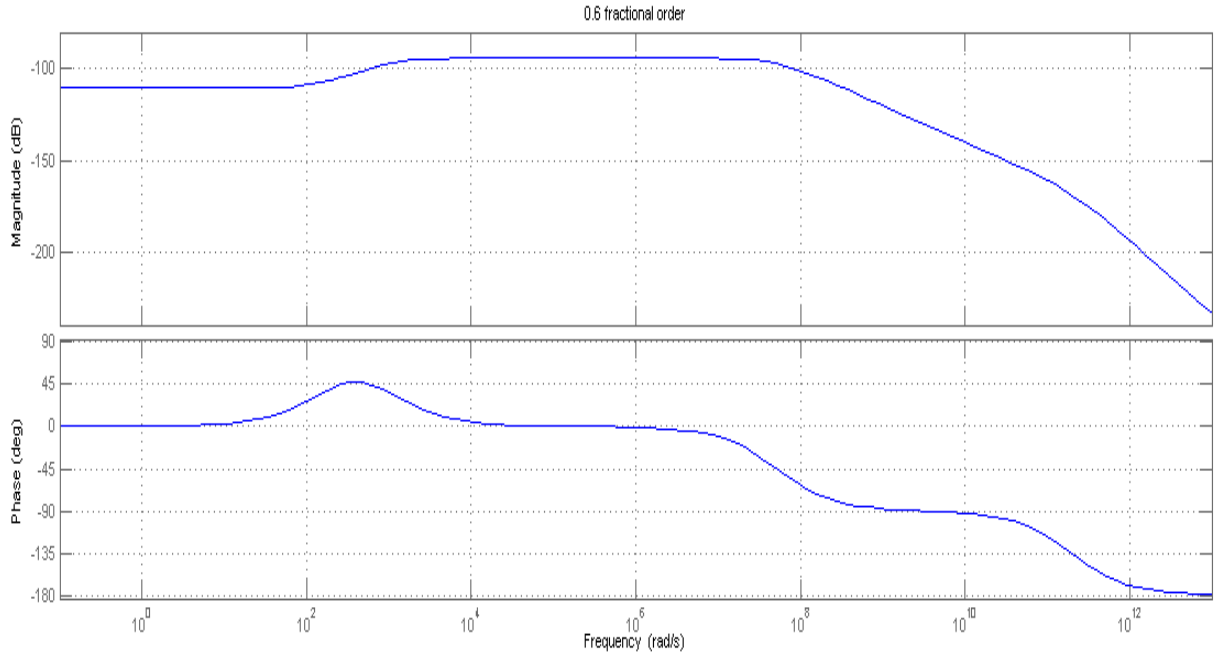
In the plot Figure.4 the frequency domain analysis is being represented in magnitude and phase of the prescribed amplifier and being analyzed for further upgradation in fractional domain.

By implementation fractional capacitor in C_1, C_2 and C_3 and by using the above sub-system Figure.1 in the Figure.2

we have,

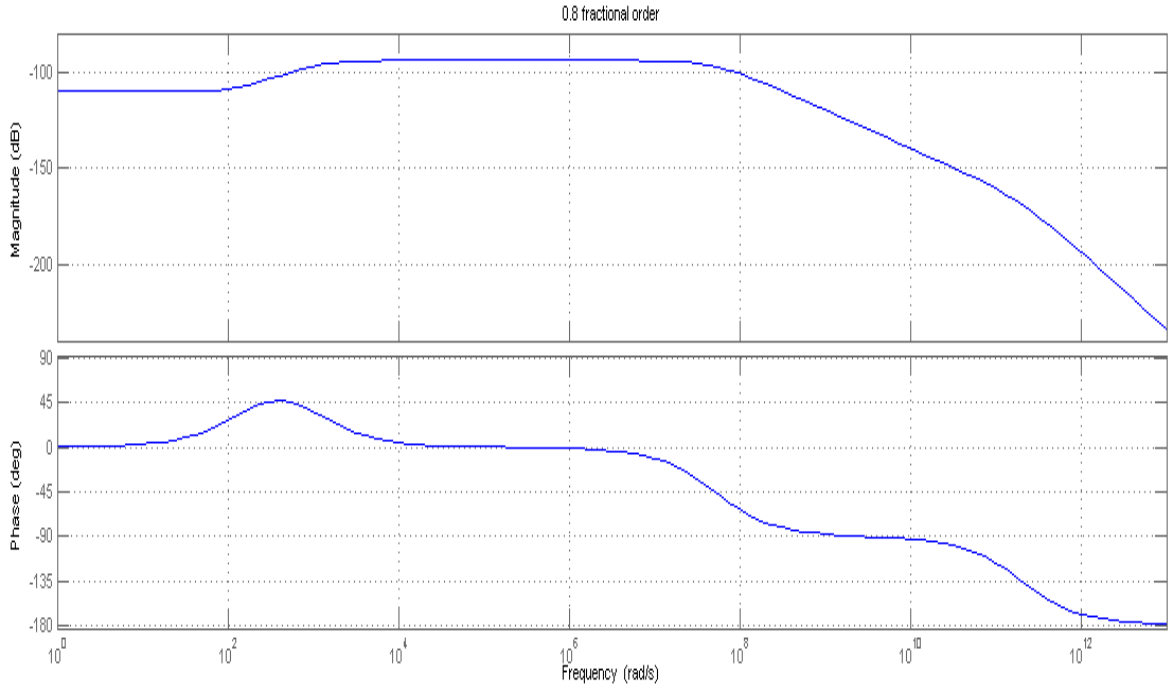


(a) Fractional 0.4 order



(b)Fractional 0.6 order.

when α value will be equal to 0.6 then the bandwidth will be nearly equal to the bandwidth of integer order amplifier



(c) Fractional 0.8 order.

when α value will be equal to 0.8 then the bandwidth will be maximum and it will give flatted response

Figure.6 Magnitude and phase plots of fractional order RC based amplifier at different orders.

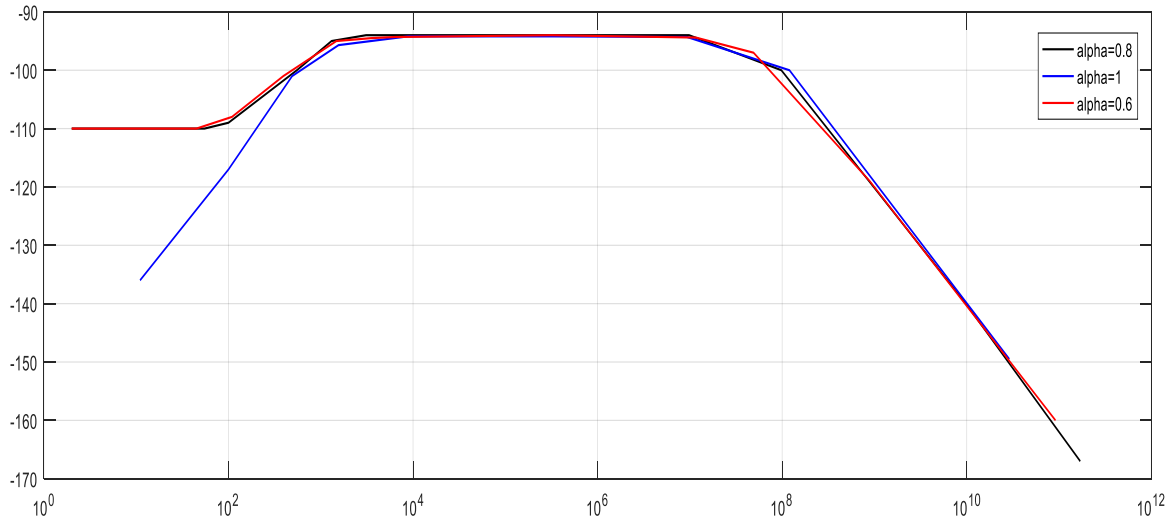


Figure.7. Comparison of integer order magnitude RC amplifier plots with fractional counterpart.

From the above figure the integer order amplifier circuit and the fractional order amplifier circuit parameters were studied

Table.3. Frequency domain analysis of fractional order BJT based amplifier a different order of α

Parameters	α =1.0	α =0.8	α =0.6
f_L *(Hz)*	926	981.6	828.2
f_H*(Hz)*	4.99 x 10^5	5.54 x 10^7	4.94 x 10^7

f_c *(Hz)*	4.49×10^4	3.1×10^5	1.3×10^6
t_r *(Hz)*	4.99×10^4	6.48×10^4	7.14×10^4
Bandwidth (Hz)	4.98×10^7	5.4×10^7	$4.93\ \ 10^7$

V. CONCLUSIONS

From, the above analysis first the passive symmetric design of fractional capacitor is being designed in MATLAB R2016a Simulink, the required passive channel was being reated using the specified resistors and capacitors as mentioned in Table.2 and being generalized of fractional orders nearer to the integer order i.e. 0.6 and 0.8. Then, experimentally the domino ladder circuit is being implemented in breadboard circuit using the required resistors and capacitors for satisfying the order of α=0.8. The output to the sine wave is being generalized using Zelscope oscilloscope and being figured in fig2(a) and Figure.2(b). Where, the phase shift is being observed at -71.6 which when calculated in equation 9 evaluated to the value of α=0.796.

A RC coupled BJT based amplifier is being designed in Simulink and the frequency domain analysis is being carried out where the magnitude and phase is plotted and the frequency domain analysis is tabulated. The specified fractional capacitor designed in the Simulink earlier is then imprinted in the RC coupled amplifier and the plots of frequency domain is being obtained and compared with the classical amplifier in integer domain.

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