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Digital Clock Frequency Multiplier Using Floating Point Arithmetic

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Abstract— A digital clock frequency multiplier using floating point arithmetic, which generates the output clock with zero frequency error has been presented. The circuit has an unbounded multiplication factor range and low lock time. A low power mechanism has been incorporated to ensure that the overall power consumption of the circuit is less. The circuit has been designed in TSMC 65nm CMOS process for an input reference time of 0.01ns and has been verified with random multiplication factor values.

Keywords— Frequency multiplier, floating point, CMOS, PLL

I. INTRODUCTION

Clock frequency multipliers are widely used in Integrated Circuits. Conventionally, phase locked loops (PLLs) [1, 2] are used as clock frequency multipliers to increase the frequency of an input clock signal. However, PLLs require much time and design efforts to ensure stability. And also PLLs consume large silicon area and often require different external components for usage, resulting in high cost. Because of high lock time of PLL, the input clock signal frequency cannot be changed quickly. PLLs are only suited for handling input clock signals of limited frequency and duty cycle ranges, and individual PLLs have limited multiplication ranges.

The other method of multiplying the frequency is to convert the input frequency to an analog voltage, process the voltage using op-amp, and then convert the processed voltage to a higher frequency using a V/F converter. At low frequencies, the Frequency to Voltage converter cannot produce a steady voltage output. A large amount of ripple is produced which may be easily eliminated using DC filters, but the response time of the system becomes very high which is unacceptable.

Extensive work has been done on building clock multipliers and different circuits have been proposed [3]. Still, the major consideration while implementing clock multipliers will be, to improve the accuracy of the output clock frequency value as much as possible. This issue is being addressed in this paper.

The proposed architecture attempts to address the above mentioned issues associated with both PLLs and F/V-V/F converters. It has a wide multiplication factor range and can generate an output clock with an accurate frequency. The architecture is stable because of open loop characteristics [4].

The proposed architecture can be used with an input signal of any duty cycle varying from 10-90% and with any multiplication factor.

The rest of paper is organized as follows: Section 2 gives the design algorithm of the digital clock frequency multiplication. Section 3 discusses about the digital clock frequency multiplier which has been developed using the proposed algorithm. Simulation and synthesis results for programmable digital frequency multiplier [3] and the suggested digital clock frequency multiplier have been presented in section 4 and section 5 respectively. Last section presents the conclusion.

II. DESIGN ALGORITHM

The existing algorithm [3] for clock frequency multiplication is based on determining the time period of input clock signal with a high frequency. In order to determine an accurate value of the input clock signal time period, a very high frequency clock (>1GHz) should be used, which in turn requires a high frequency clock generation circuit. If the input clock signal and high frequency signal are from different sources, then a synchronizing circuit is required to reduce the phase difference between the clock and high frequency signal.

In the proposed digital clock frequency multiplier, instead of a high frequency signal, a reference time is used to determine the time period of the input clock signal. The algorithm of the proposed frequency multiplier is as follows:

1. Receive an Input clock signal which has to be multiplied, the multiplication factor (MF) and the reference time.
2. With the help of reference time, determine Total time period, ON time and OFF time of an input clock signal.
3. Convert the obtained time periods (from step 2) and Multiplication factor (MF) to the IEEE 754 standard format.
4. By using floating point division algorithm, divide the time periods (from step 3) with the multiplication factor (MF) in order to determine the required Total time period, ON time period and OFF time period of output clock signal. Equations for the required total time period (T), ON period and OFF period of output clock signal are given below.

$$T_{Clock\_Out} = T_{Clock\_In}/MF \quad (1)$$

$$T_{Clock\_Out(ON)} = T_{Clock\_In(ON)}/MF \quad (2)$$

$$T_{Clock\_Out(OFF)} = T_{Clock\_In(OFF)}/MF \quad (3)$$

5. With the help of reference time, generate an output clock signal with determined Total time period, ON time and OFF time (from step 4).

By using the above algorithm, we can overcome the addition of high frequency signal generators and synchronizing circuits to the clock frequency multiplier circuit. The digital logic which implements the above algorithm is discussed in the following section.

III. BLOCK DIAGRAM DESCRIPTION

Figure 1 shows the block diagram of the proposed clock frequency multiplier using floating point arithmetic. The circuit consists of a time period determination circuit, multiplexer, a floating point division unit, de-multiplexer, an output clock generation circuit and a controller [5].

Inputs for the time period determination circuit are, the clock signal that has to be multiplied and the reference time, using which the total time period, ON time and OFF time of input clock signal is determined. The time determination circuit is a combination of adders and comparators. Once the total time, ON time and OFF time are determined, they are converted to the IEEE 754 standard single precision format [6] and stored in the internal registers before disabling the enable signal for the time period determination circuit

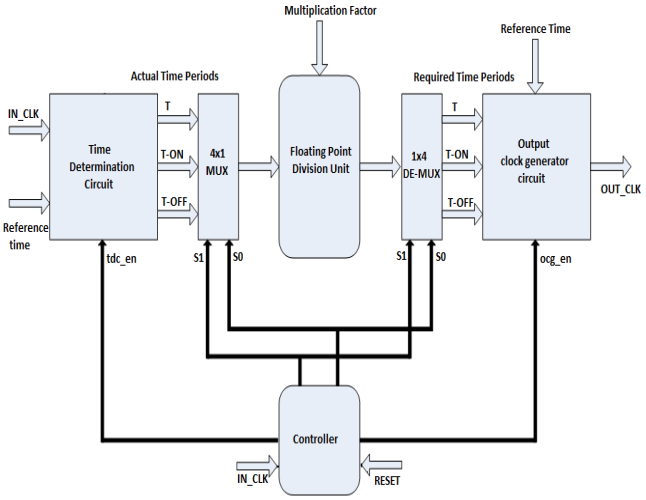

Figure 1: Block diagram of the Clock frequency multiplier using floating point arithmetic

The next block after the time period determination circuit is the point divider unit [6]. The floating point divider unit will receive the multiplication factor, convert it to the IEEE 754 standard single precision format [6] and divide the determined time periods to generate the required total time period, ON time and OFF time.

Instead of using 3 floating point dividers each for determined total time, ON time and OFF time respectively, a single floating point divider is used and the determined time periods from the time period determination circuit are passed through the divider one by one to calculate the required time period of the output signal. Controller block controls the above process of sending each time period value at a time through the floating point divider [6]. By using the above process, the gate count and power corresponding to the redundant divider logic can be reduced to a large extent.

In the proposed digital clock frequency multiplier, the multiplication factor (MF) is not restricted to any specific range as in the programmable digital frequency multiplier [3]. Also, the MF in the proposed architecture can be a floating point value like 0.5, 2.5, 12.3 and so on.

The output clock generator circuit receives the required total time period, ON time, and OFF time values from the floating point divider unit [6]. In the output clock generator, the reference time is given as an input to a floating point adder [6, 8], wherein the output is connected as one of the inputs. The output of the floating point adder [6, 8] is compared with the required total time, ON time and OFF time values which are determined from the floating point divider unit [6].

Initially, outputs of the output clock generator circuit and the floating point adder [6, 8] are zeros. Once the addition process starts, output of the floating point adder [6, 8] is given to the comparator circuit. When the output of the floating point adder is equal to the required OFF time, the output clock signal is toggled from zero to one and when the adder output is equal to the required ON time, the output clock signal is toggled from one to zero. When the output of the floating point adder is equal to the required total time period, its output value will be reset to zero, output clock signal will be toggled from zero to one and the process repeats.

The controller block generates the enable signals (tdc_en, ocg_en) and select lines (s_0 and s_1) for the time determination circuit, output clock generator circuit and 4x1 multiplexers respectively. The controller is designed in such a way that, at any instant of time, only one of the 3 sections will be enabled. Since only one unit will be working at any time instant, the overall power consumption of the proposed architecture is less when compared to the programmable digital frequency multiplier in [3].

The circuit has a deterministic lock time of 8 clock cycles. If the input clock frequency changes, then the corresponding output clock frequency will appear after 8 clock cycles of the input clock.

IV. SIMULATION RESULTS

Figures 2 and 3 show the simulated output waveforms for both, the programmable digital frequency multiplier [3] and the proposed digital clock frequency multiplier respectively with MF=40.

It is clear from figures 2 and 3 that when an asymmetric input signal with 25-75% duty cycle is given to the proposed digital clock frequency multiplier, the output signal will also have the same duty cycle as that of the input. But, when the same input signal with 25-75% duty cycle is given to the programmable digital frequency multiplier, the output signal is still symmetric.

Figure 4 shows the simulated output waveforms of the proposed digital clock frequency multiplier with MF=0.5 and an input frequency of 12MHz. The proposed architecture has been simulated with random Multiplication Factors and also different input signals with random duty cycles.

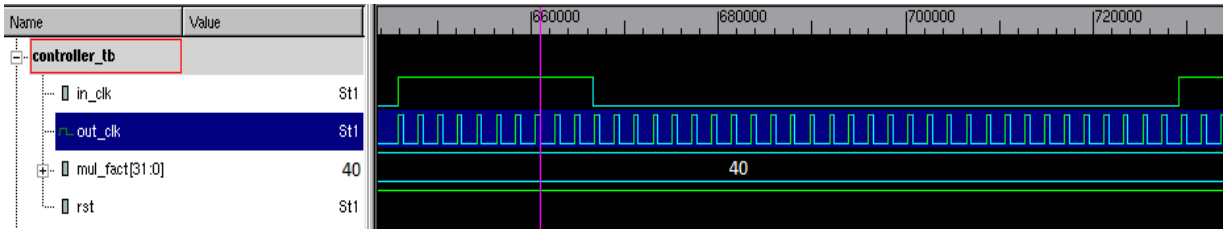

Figure 2: Simulation result of proposed frequency multiplier with asymmetric input clock with MF = 40

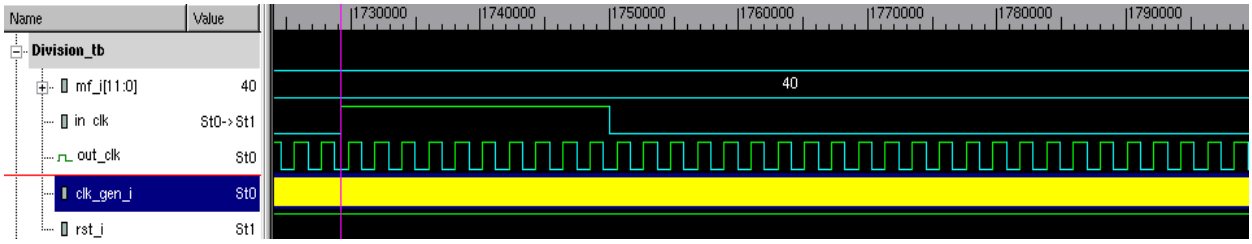

Figure 3: Simulation result of programmable frequency multiplier with asymmetric input clock with MF = 40

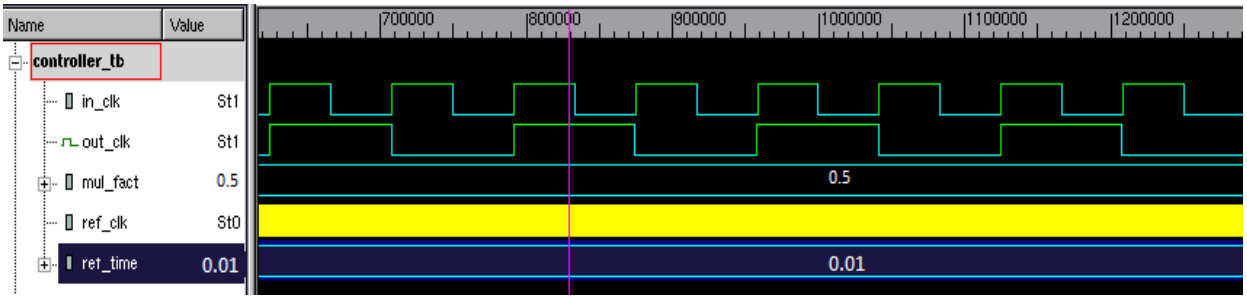

Figure 4: Simulation result of proposed frequency multiplier with MF = 0.5

V. SYNTHESIS RESULTS

The proposed circuit and the programmable digital frequency multiplier [3] have been coded using generic Verilog HDL and are synthesized using the Synopsys Design Compiler with TSMC 65nm technology library.

Table 1 shows the difference in the synthesis results between the programmable digital frequency multiplier [3] and the proposed digital clock frequency multiplier.

Table 1. Synthesis results of Digital frequency multipliers

Parameters	Programmable Digital frequency multiplier	Proposed Digital clock frequency multiplier
Area	4310.64	5422.3
Dynamic power	1.548 mW	0.7 mW
Cell Leakage power	142.255 uW	88.34 uW
Lock time	12 clock cycles	8 clock cycles

From Table 1, it can be observed that the proposed digital clock frequency multiplier has less lock time when compared to the programmable digital frequency multiplier [3]. While considering the area, the proposed digital clock

frequency multiplier will occupy more area when compared to the programmable digital frequency multiplier [3]. The low lock time and low power can be compromised with a smaller area.

VI. CONCLUSION

This paper describes the design of a digital clock frequency multiplier using floating point arithmetic. The new proposed clock frequency multiplier has the shorter lock time when compared to the programmable digital frequency multiplier, which has been examined in this paper. The new clock frequency multiplier improves the accuracy of frequency multiplication by using the floating point division algorithm. The clock frequency multiplier has been designed using Verilog HDL and verified for different corner case inputs. Also, the proposed clock frequency multiplier has been synthesized with TSMC 65nm CMOS library

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