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FPGA Implementation of a 4×4 Vedic Multiplier

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Abstract:- this paper portrays for the design of an area efficient 4×4 Vedic Multiplier by using Vedic Mathematics algorithms. Out of the 16 sutras the Urdhva -Tiryakbhyam sutra is being discussed and implemented because this sutra is applicable to all cases of algorithm for n×n bit numbers and gives minimum delay for multiplication of all types of numbers. The complete multiplier is designed using VHDL language. The design is simulated using Xilinx ISE project navigator and the functionality of the circuit is verified by generating test-bench waveform. The proposed multiplier in this paper can be used in many real-time signal and image processing applications.

Keywords:- Very high speed integrated circuit (VHSIC); VHSIC hardware description language (VHDL); Vedic Mathematics; Vedic Multiplier; Urdhva –Tiryakbhyam (UT).

I. INTRODUCTION

MATHEMATICS is mother of all sciences. Mathematics is full of magic and mysteries. The ancient Indians were able to understand these mysteries and develop simple keys to solve these mysteries. Thousands of years ago the Indians used these techniques in different fields like construction of temples, astrology, medical science etc., due to which INDIA emerged as the richest country in the world. The Indians called this system of calculations as **"THE VEDIC MATHEMATICS"**. Vedic Mathematics is much simpler and easy to understand than conventional mathematics [5].

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code [5].

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier [4]. Employing this technique in the computation algorithms will reduce the complexity, execution time, power etc.

The 16-Vedic Sutras along with their brief meanings are enlisted below alphabetically [5].

1) (Anurupye) Shunyamanyat - If one is in ratio. The other is zero
2) Chalana-Kalanabyham Differences and Similarities.
3) Ekadhikina Purvena - By one more than the previous one
4) Ekanyunena Purvena - By one less than the previous one
5) Gunakasamuchyah - The factors of the sum is equal to the sum of the factors
6) Gunitasamuchyah - The product of the sum is equal to the sum of the product
7) Nikhilam Navatashcaramam Dashatah - All from 9 and the last from 10
8) Paraavartya Yojayet - Transpose and adjust.
9) Puranapuranabyham - By the completion or Non-completion
10) Sankalana-vyavakalanabhyam - By addition and by subtraction
11) Shesanyankena Charamena - The remainders by the last digit
12) Shunyam Saamyasamuccaye - When the sum is the same that sum is zero
13) Sopaantyadvayamantyam - The ultimate and twice the penultimate
14) Urdhva -Tiryakbhyam - Vertically and crosswise
15) Vyashtisamanstih - Part and Whole

16) Yaavadunam - Whatever the extent of its deficiency

A high speed energy efficient ALU design using Vedic mathematics is discussed in [1]. They have implemented ALUusing adder, subtractor, Vedic multiplier, and MAC unit. They have implemented MAC using Vedic multiplier. Their Vedic multiplier architecture shows speed improvements over conventional shift and add algorithm.

In [2], authors have compared implementation of normal multiplication and Vedic multiplication. They claim that same
number of multiplication and addition operations is required in
both normal multiplier and Vedic multiplier. They have tested
and compared various multiplier implementations such as Array multiplier, Multiplier macro, Vedic multiplier with full
partitioning, Vedic multiplier using 4 bit macro, fully Recursive Vedic multiplier, Vedic multiplier using 8 bit macro for optimum speed.

Dhillon and Mitra [3] proposed a multiplier using "Urdhva Tiryagbhyam" algorithm, which is optimized by "Nikhilam" algorithm. They have suggested a reduced bit multiplication
algorithm using "Urdhva Tiryagbhyam" and "Nikhilam Sutra". Their multiplier architecture is very similar to the array
multiplier.

This paper is organized as follows; Section **II** is reviewing the theoretical background and operation principle of **Urdhva -Tiryakbhyam**. In Section **III** the brief description of design flow of various models and sub models are given. Section **IV** carries the result discussion and at last conclusion is given in Section **V**.

II .PROPOSED TECHNIQUE

URDHVA -TIRYAKBHYAM:-

Urdhva-Tiryakbhyam means vertical and crosswise multiplication. This sutra is a general multiplication formula applicable to all cases of algorithm for n×n bit numbers [6]. The partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The advantage of this multiplier is that as the number of bits increases, delay and area increases very slowly as compared to other multipliers.

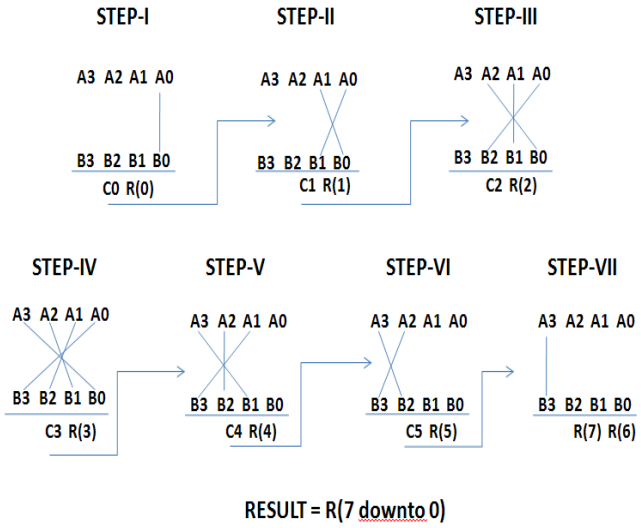

Figure.1(a) Multiplication method of Urdhva-Tiryakbhyam

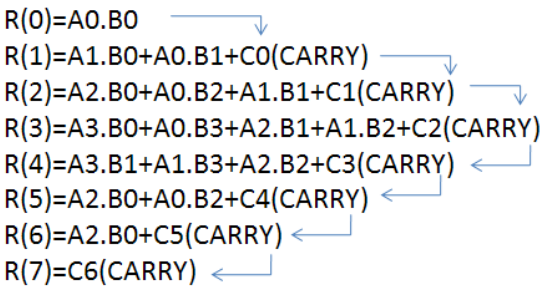

Figure.1(a) Equations used for designing a 4×4 Vedic-Multiplier

III. DESIGN DESCRIPTION

In this project work all the designs are done using VHDL language. VHDL is an acronym for VHSIC (Very High Speed Integrated Circuit) Hardware Description Language. It is intended for documenting and modeling digital systems ranging from a small chip to a large system. VHDL is used because of its portability, flexibility, and readability. The design of each block includes the following steps 1.Understanding the functionality of the module and its sub-modules, 2.Developing VHDL codes for the top module and its sub-modules, 3.Design synthesis, 4.Mapping and Routing, 5.Test-bench waveform generation and testing, 6.Error-correction, 7.FPGA Implementation. In this project all the designs have been implemented on an Spartan 3E family FPGA using the Xilinx 10.1 ISETM design tool suite.

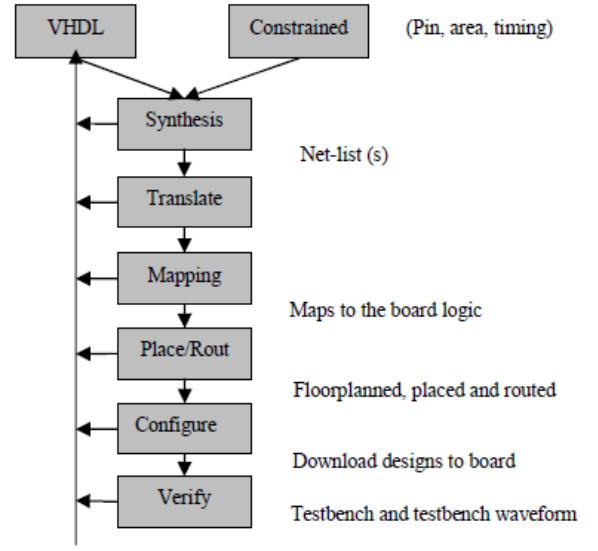

Figure 2 –Xilinx 10.1 ISE tool design flow

TABLE I

FPGA SPECIFICATION	
FAMILY	**Spartan 3E**
DEVICE NAME	**XC3S500E**
PACKAGE	**PQ208**
SPEED GRADE	**-4**

IV. RESULT & DISCUSSION

In this part the RTL-Schematic, Testbench Waveform, Design Utilization summary, delay report etc. are shown, which are generated using Xilinx ISE project navigator.

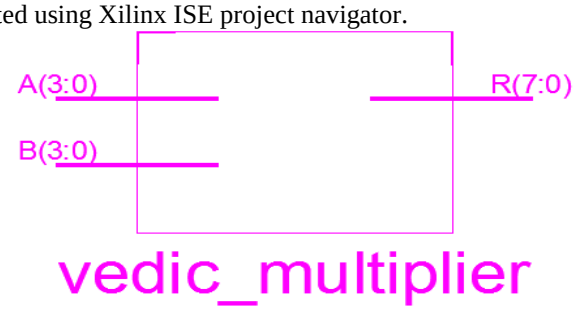

Figure 3 –RTL Schematic1

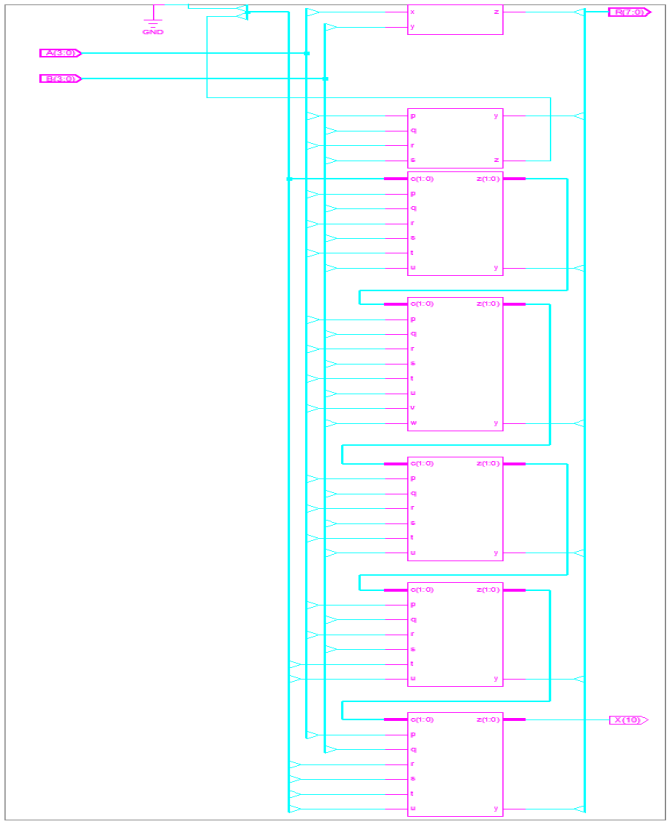

Figure 4 –RTL Schematic2

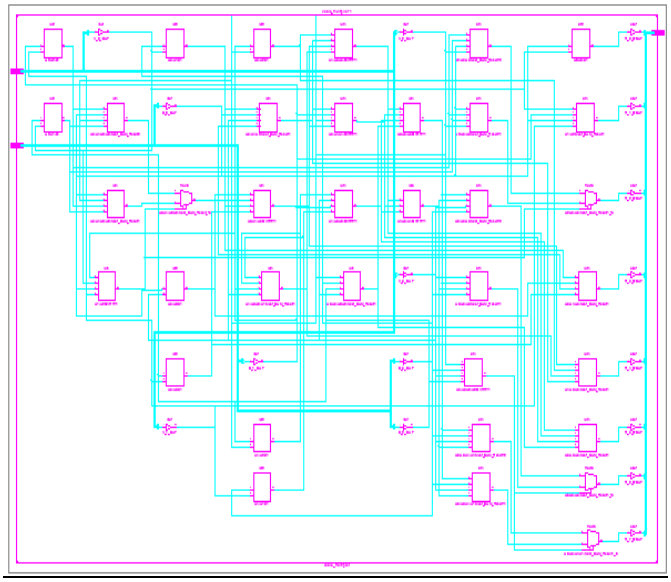

Figure 5 –Technology Schematic

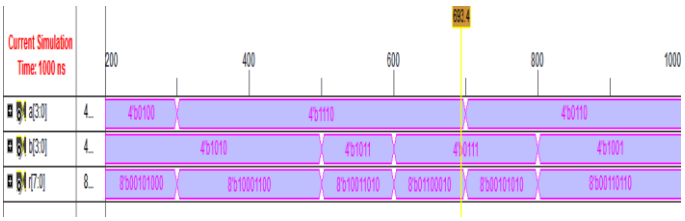

Figure 6 –Testbench Waveform

TABLE II.

DESIGN UTILIZATION SUMMARY FOR VEDIC MULTIPLIER			
parameter	**used**	**available**	**% of Utiliza-tion**
Number of Slices	**24**	**4656**	**0%**
Number of 4 input LUTs	**42**	**9312**	**0%**
Number of bonded IOBs	**16**	**158**	**10%**

TABLE III

DELAY REPORT	
Total fanout	**33**
Total Gate Delay	**10.122ns**
Total Net Delay	**5.759ns**
Total combinational path delay	**15.881ns**

V. CONCLUSION

The Vedic Multiplier is designed using VHDL language. Each block and its sub-blocks are tested separately and the errors are corrected. Test-bench waveforms are generated for each sub-block of system and its functionality is verified. The result shows that the proposed design use less amount of the hardware resources and shows total 15.881ns delay, which is very less.

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