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Low Power Wide Frequency Range Current Starved CMOS VCO in 180nm, 130nm and 90nm CMOS Technology

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Abstract:- This paper describes a design and implementation of Five Stage Current Starved CMOS Voltage Controlled Oscillator for Phase Locked Loop. Current starved VCO is simple ring oscillator consisting of cascaded inverters.The performance comparision is done with repect to power dissipation and phase noise characteristics for three different technology The design is implemented in Mentor Graphics using ELDO SPICE simulator with high oscillation frequency, low power consumption, and low area.

Keywords:- Current starved VCO, oscillators, phase noise, Source Coupled VCO, ring oscillators,

I. INTRODUCTION

A CMOS Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. VCO constitute a critical component in many RF transceivers and are commonly associated with signal processing tasks like frequency selection and signal generation. RF transceivers of today require programmable carrier frequencies and rely on phase locked loops (PLL) to accomplish the same. These PLLs embed a less accurate RF oscillator in a feedback loop, whose frequency can be controlled with a control signal. Transceivers for wireless communication system contain low-noise amplifiers, power amplifiers, mixers, digital signal-processing chips, filters, and phase-locked loops.
Voltage controlled oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency Circuits. Their output frequency is a function of a control input usually a voltage. An ideal voltage-controlled voltage oscillator is a circuit whose output frequency is a linear function of its control voltage. Most application required that oscillator be tunable, i.e. their output frequency be a function of a control input, usually a voltage.

There are two different types of voltage controlled oscillators used in PLL, Current starved VCO and Source coupled VCO [1].In recent years LC tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages. First, the tuning range of an LC-oscillator (around 10 - 20%) is relatively low when compared to ring oscillators (>50%). So the output frequency may fall out of the desired range in the presence of process variation. Second, the phase-noise performance of the oscillators highly depends on the quality factor of on-chip spiral inductors. For most digital CMOS processes, it is difficult to obtain a quality factor of the inductor larger than three. Therefore, some extra processing steps may be required.

The ring oscillators, however, do not have the complication of the on-chip inductors required for the LC oscillators. Thus the chip area is reduced. In addition to a wide tuning range; ring oscillators with even number of delay cells can produce quadrature-phase outputs [3]. The phase noise performance of ring oscillators is much poorer in general [8], [4]. Also, at high oscillation frequencies, the power consumption of the ring oscillators may not be low which is a key requirement for battery operated devices [10]. To overcome these problems, we work on five stages current starved Oscillator without an LC tank. Finally performances are compared based on their results in different Technology.

II. CIRCUIT DESCRIPTION

The operation of current starved VCO is similar to the ring oscillator. Fig 1. Shows a five stage Current-Starved VCO [5].Middle PMOSM1 and NMOSM2 operate as inverter, while upper PMOSM13 and lower NMOSM14 operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. PMOSM22 and NMOSM21 drain currents are the same and are set by the input control voltage . Fig 2 shows the inverter schematic [5]. The inverter sizes PMOS22 and NMOS21, of Fig.2, are calculated.

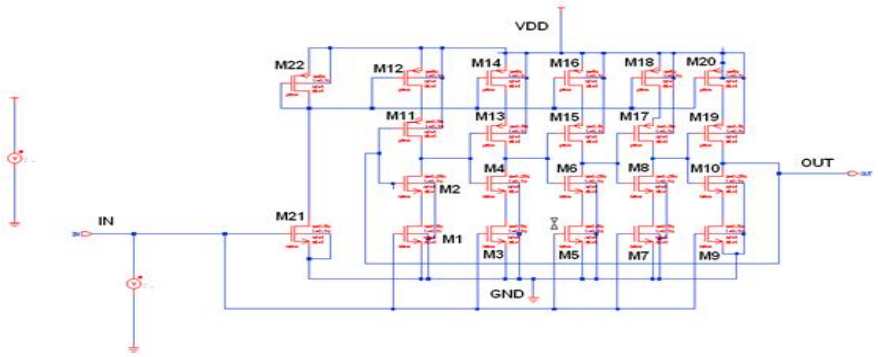

Fig 1: Current Starved CMOS Voltage Controlled Oscillator in IC Schematic Editor

The total capacitance Ctot is given by,

$$C_{tot} = \frac{5}{2} C_{ox}^{'}(W_p L_p + W_n L_n) \quad (1)$$

Where Cox is the oxide capacitance.

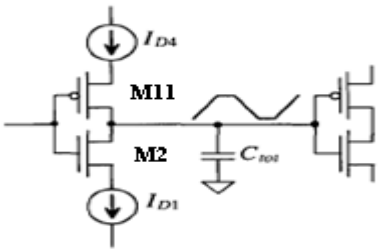

Fig 2: Inverter Schematic

The number of stages of the oscillator is selected; there are 5 stages. The centre drain current is calculated as:

$$Iavg = N\frac{VDD.Ctot}{T} = N.VDD.Ctot.Fosc \quad (2)$$

Where N is the number of stages of inverter. The sizes of PMOS22 and NMOS21 are determined as:

$$Idcentre = \frac{\beta(Vgs-Vt}{2} \quad (3)$$

Where, $\beta = Kp * W/L$, it can be shown that the oscillation frequency is:

$$F_{osc} = \frac{1}{N(t_1+t_2)} = \frac{I_D}{N.C_{tot}.VDD} \quad (4)$$

=Fcen@VinVCO (5)

Where Td is the time delay above equation gives the centre frequency of the VCO when ID=IDcentre. The VCO stops oscillating, neglecting sub threshold currents, When, VinVCO<Vthn.Thus, Vmin=Vthn and Fmin=0. The max VCO oscillation frequency Fmax is determined by Finding ID when VinVCO=VDD. At the max frequency then, Vmax=VDD.

III. SIMULATION RESULTS

A. Implemented in 180nm CMOS Technology

Table 1: Simulated Results for Current Starved CMOS VCO in 180nm Technology

Control Voltage (V)	Oscillating Frequency(MHz)
0.6	165.23
0.7	438.94
0.8	754.46
0.9	1061.4
1.0	1333.0
1.1	1562.0
1.2	1762.8
1.3	1926.5

1.4	2041.5
1.5	2118.9
1.6	2200.1
1.7	2247.7
1.8	2307.5

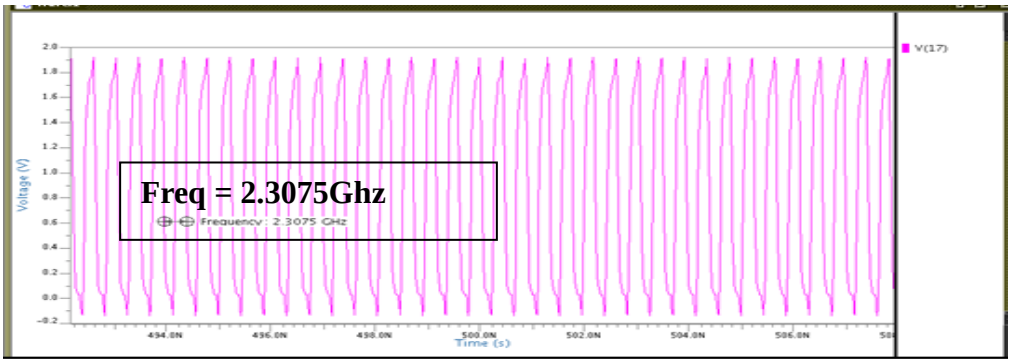

Fig 3: Output Waveform for 1.8v Control Voltage of Current Starved VCO in 180nm Technology.

B. Implemented in 130nm CMOS Technology

Table 2: Simulated Results for Current Starved CMOS VCO in 130nm Technology

Control Voltage (V)	**Oscillating Frequency(MHz)**
0.1	28.237
0.2	154.11
0.3	512.90
0.4	938.95
0.5	1356.5
0.6	2206.2
0.7	2801.0
0.8	3150.0
0.9	3317.9
1.0	3392.3
1.1	3477.9
1.2	3539.9
1.3	3588.8

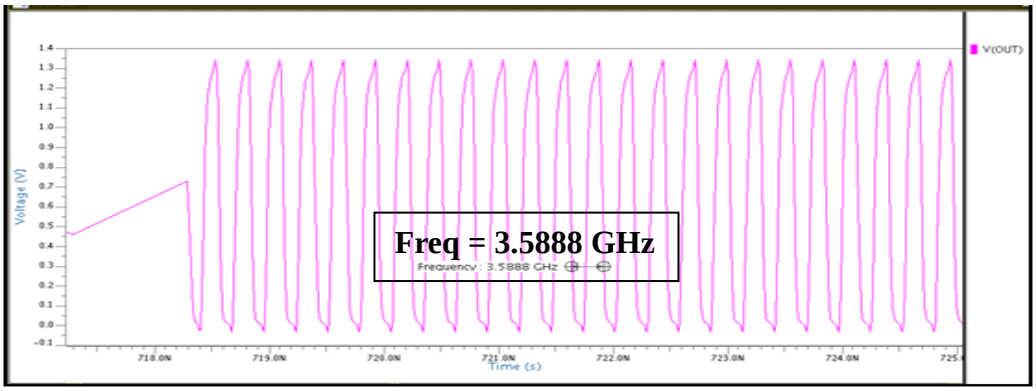

Fig 4: Output Waveform for 1.3v Control Voltage of Current Starved VCO in 130nm Technology.

C. Implemented in 90nm CMOS Technology

Table 3: Simulated Results for Current Starved CMOS VCO in 90nm Technology

Control Voltage (V)	**Oscillating Frequency(MHz)**
0.100	50.00
0.150	99.785
0.200	193.91

0.250	350.00
0.300	588.53
0.350	938.95
0.400	1373.4
0.450	1818.6
0.500	2226.8
0.550	2557.9
0.600	2799.2
0.650	2974.1
0.700	3104.4
0.750	3205.0
0.800	3285.2
0.900	3405.0
1.00	3513.4

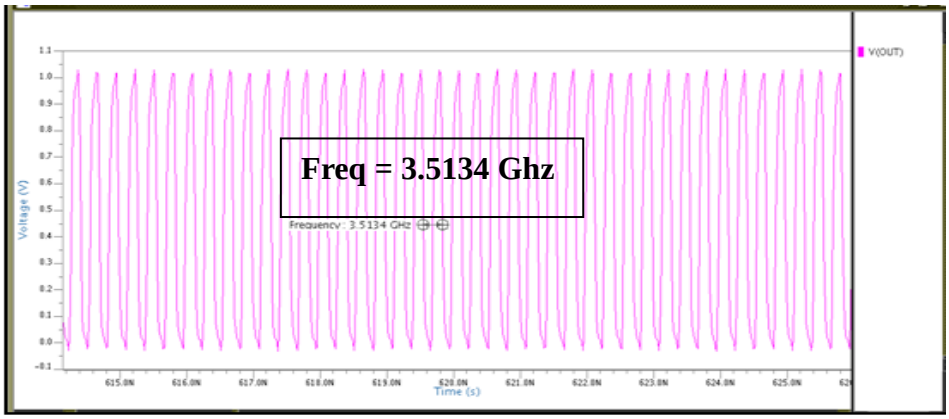

Fig 5: Output Waveform for 1v Control Voltage of Current Starved VCO in 90nm Technology.

The performance comparision in terms of power dissipation, oscillating frequency, and phase noise, for Five stages current starved CMOS VCO in three differnet Technology is as shown in Table 4.

Table 4: Summary of Results for Current Starved CMOS VCO in Different Technology

Parameters	**In 180 nm**	**130 nm**	**In 90 nm**
Power Supply (V)	1.8	1.3	1
Frequency Range	165.23MHz - 2.3073GHz	28.237MHz - 3.5888GHz	50MHz – 3.5134GHz
Phase Noise (dBc/Hz @ 1MHz)	-124.52	-118	-116
Power Dissipation (µW)	1235.7	590.88	240

IV. CONCLUSIONS

This paper shows the Five stages current starved CMOS VCO simulated in ELDO SPICE simulator having low power dissipaton and phase noise as compare to LC oscilator.By observing the Table 4, it can be concluded that the phase noise characteristics of CMOS VCO get worst as we scale down into the Technology node.While the power dissipation of this oscillator will decrease as we go scale down to the Technology node.This circuit is having the application in PLL for low power and low phase noise peformance requirements.

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