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Quasi-Three-Level and Five-Level Operation of A Diode-Clamped Multilevel Inverter Using Space Vector Modulation

[1]k.Rajesh, [2]k.Vijaya Bhaskar,
[1]*PG student (PE&ED), S.V.P.C.E.T., Puttur,*
[2]*Associate Professor,S.V.P.C.E.T., Puttur,*

Abstract:- This study presents space vector-based quasi-two-level operation of a diode-clamped multilevel inverter which improves dc link utilisation and output voltage quality, and avoids the dc link capacitor voltage balancing problem experienced with standard multilevel operation. Beside a review of quasi-two-level operation and the capacitor voltage balancing method, the study presents a detailed discussion on the implementation of space vector modulation and the selection of switching sequence for a five-level inverter. Additionally, the condition for maximum theoretical modulation index for space vector modulation is established. A prototype five-level diode-clamped inverter is to experimentally validate the approach. Also this study extends the concept of quasi-two-level-to-three-level operation of the diode-clamped multilevel inverter in order to address the shortcomings experienced with quasi-two-level operation, such as low waveform quality and high switching losses. The validity of three-level inverter operation is confirmed experimentally on a prototype of a five-level diode-clamped inverter. The study also highlights the limitations of three-level operation of a diode-clamped multilevel inverter.

I. INTRODUCTION

Two-level voltage source inverters are commonly used in many applications, ranging from low voltage to high voltage [1]–[5]. In medium- and high-voltage applications, two-level converters with series connected devices are preferred because of its simple construction, simple to control and resilience to ac faults. However, they require large ac filters and transformers with high insulation requirements owing to increased dv/dt (resulting from switching a large voltage step) and have higher switching losses [4]–[9]. The alternative approach for generating high voltage is to use a multilevel converter [8]. This approach reduces the filtering requirements (requires small ac filters), generates high voltage without the need for series connection of the devices, reduces insulation requirements on the interfacing transformer owing to low dv/dt (resulting from the switching of small voltage step at reduced switching frequency) and have lower switching losses [9]–[19]. However, the device count and complexity of the control system increase significantly; ability to ride through different types of faults is in doubt and requires complex capacity voltage balancing methods, which increase with the number of levels. The common types of multilevel converters are diode-clamped, flying capacitors, cascaded with an electrically isolated dc source and a modular converter [20]-[21]. Diode-clamped multilevel inverters have received more research and industrial attention than other multilevel topologies. This is because of its unique circuit structure that allows regeneration (bi-directional power flow) at no addition cost; requires fewer capacitors (resulting in small size) and the device voltage stress is limited to one capacitor voltage. In order to sustain these advantages, the voltage across each dc link capacitor of the diode-clamped circuit must be maintained at Vdc/(N 2 1), where N is the number of levels and Vdc is rail-to-rail dc voltage [1]–[6]. The structure has higher stray inductance than other multilevel topologies.

As the number of inverter levels increases, dc link capacitor voltage balancing becomes challenging; being power factor-and modulation index-dependent [1]-[6]. This means the amount of deliverable active power and extractable voltage magnitudes are restricted depending on the inverter operating point [7]–[16]. Since a diode-clamped multilevel inverter uses the same dc link capacitors as an energy tank for the all three phases, it requires capacitor voltage balancing strategies that consider the interactive effect of the all three phases.

There are three approaches commonly used to maintain capacitor voltage balance. The first approach utilizes the addition of small dc offset to the modulating signals of the three phases in order to achieve voltage sharing between the dc link capacitors of the diode-clamped inverter [12]-[15]. However, this approach is viable only in three-phase systems where the dc offset is cancelled in the line-to-line voltage and no dc will appear in the three-phase load currents. This approach has been established only for three-level diode-clamped inverters [known as the neutral-point clamped (NPC) inverter] and limits the maximum attainable modulation index to 1 2 d, where d is the per unit dc offset demonstrate the possibility of using dc offset to balance the dc link capacitors of the active NPC converter with more than three level. However, the main drawback of the active

NPC converter with more than three levels is that it requires a number of series-connected switching devices in the inner clamping paths and in the main converter arm. In practice, this may necessitate the use of voltage sharing mechanism such as active or passive snubber circuits, which is undesirable. Also it lacks modularity as the converter switches are rated differently as they experience different voltage stresses. The authors in [25] propose an optimized pulse pattern to achieve near uniform distribution of switching losses between the converter switches, hence facilitating an approximately modular thermal circuit design. However, the authors have not addressed the problems related with series device connection. This may limit the active NPC converter to medium-voltage applications.

The second balancing approach uses the redundant state vectors of the multilevel space vector modulation that generate the same line-to-line voltage with opposite effect on the dc link capacitors of the diode-clamped inverter [6]-[19]. As the number of inverter levels increases, the usable redundant states that guarantee voltage balance, with minimum number of switching transitions within one switching cycle, tend to move towards the centre of the space vector diagram (in the area corresponding to lower modulation index) [6]-[16]. This limits the maximum achievable modulation index and results in poor harmonic performance. Also with increased levels, the number of redundant states increases exponentially, making the use of space vector modulation impractical.

The third approach uses auxiliary balancing circuitry to maintain the correct voltage sharing between the dc link capacitors [3]-[12]-[14]-[15]. This approach has been proven practically with three- and five-level inverters (single phase and three phases), however, it adds cost, losses and complexity to the control system. Since this paper is concerned with the diode-clamped inverter, the other topologies are not pursued here.

Quasi-two-level operation of a five-level diode-clamped inverter has been proposed [16]-[20] as a potential alternative to standard multilevel operation which is hampered by the capacitor voltage balancing problems. In these references, the authors use sinusoidal pulse-width modulation (SPWM) based on regular sampling. It is demonstrated that the maximum attainable modulation index for quasi-two-level operation with SPWM is 0.937 without pulse dropping for unity power factor with a dwelling time of 5 ms [16]. The key objectives of the quasi-two-level operation of a diode-clamped multilevel inverter are [16]-[20]:

- Improves the dc link voltage utilisation of the diode- clamped inverter with more than three-levels in applications involving large amounts of real power (operation with high power factor and high modulation index).
- Avoids the dc link capacitor voltage imbalance associated with standard multilevel operation.
- Instead of switching the output phase between 0 and V_{dc} a sin two-level inverter case, the intermediate nodes of the dc link capacitors are utilised to generate intermediate voltage levels; these voltage levels are used to achieve smooth transition between voltage levels 0 to V_{dc} (this reduces d_v/d_t as a result of small voltage steps). The capacitive clamps perform a controllable soft clamping function.
- Reduces dc link capacitor size, which results in lower clamping circuit stray inductance and small inverter footprint.

This paper describes the principle of quasi-two-level operation of the diode-clamped multilevel inverter where space vector modulation is used rather than SPWM. Space vector modulation is adopted in order to extend the modulation index linear range, where capacitor balancing is based on the state dwelling time. The validity of the presented results is confirmed using experimentation.

II. QUASI-TWO-LEVEL OPERATION

Fig. 1 shows one-phase of a five-level diode-clamped inverter. This diode-clamped circuit version ensures the voltages across the switching devices and clamping diodes are limited to one capacitor voltage and eliminates the need for series connection of clamping diodes. When this diode- clamped circuit is operated in quasi-two-level mode, the dc link nodes 1 – 3 are utilised to generate intermediate voltage levels in order to achieve a stepped transition between the voltage levels +1/2Vdc and -1/2Vdc, in which the intermediate voltage levels are held for minimum dwell time compatible with the recovery of the clamping circuit [16], [21] and [22]. The use of the step waveform approach within each switching cycle allows the inverter switching devices to operate based on the principle of minimum switching losses that guarantee the switching of one voltage level in each switching instant. As a result the overall d_v/d_t is reduced [16]. However, the effective switching frequency per switch is the same as the two-level inverter (this may increase the switching frequency considerably). This approach also eliminates the need for series connection of the devices and capacitive snubber circuits.

Since quasi-two-level operation does not utilise the full potential of multilevel modulation, it produces lower-quality output voltage compared to full multilevel operation for the same number of levels and switching frequency. However, it represents a practical compromise between a multilevel inverter operation and two-level inverter operation.

During the switching transition of the output voltage from 0 to V_{dc} and vice versa, the dc link nodes 1 – 3 are loaded with a short pulse current of dwell duration of Td with an average magnitude of $i_a T_d/T_s$, where i_a is

the phase current and Ts is the switching cycle. As a result, the current shape drawn from these nodes are a sampled version of the load currents as shown in Fig. 2. Since the intermediate dc link nodes (1 – 3) are used only for short durations, the energy drawn from the dc link capacitors is much smaller than with full multilevel operation; as a result, capacitor voltage balancing issues are significantly reduced.

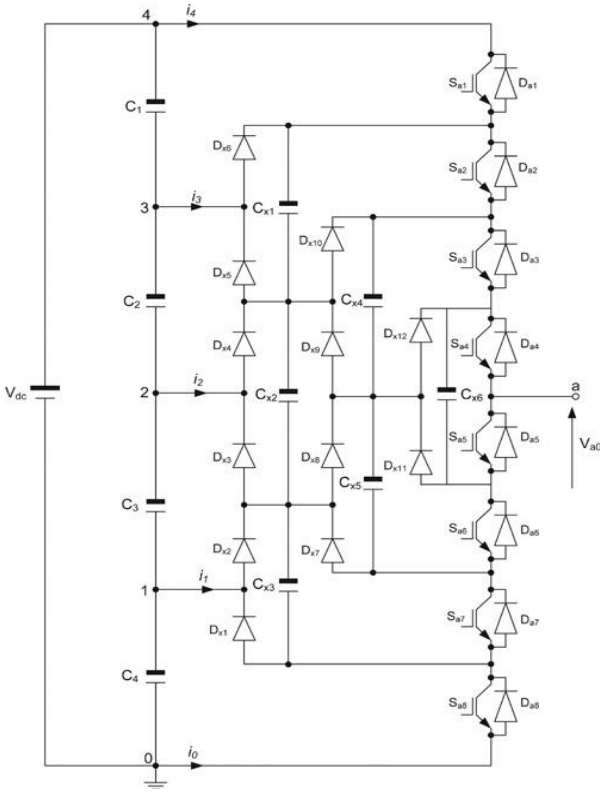
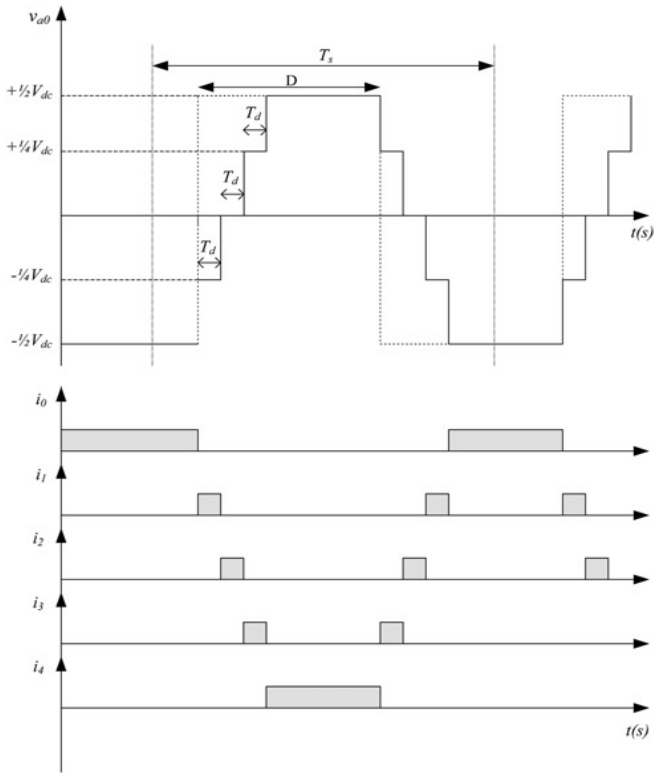
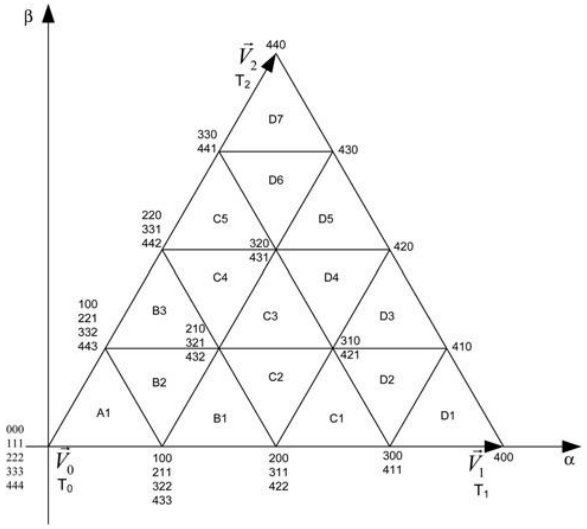


Fig.1. one-phase leg of a five-level diode-clamped inverter



III. SPACE VECTOR PULSE-WIDTH MODULATION IMPLEMENTATION OF QUASI-TWO-LEVEL OPERATION

Quasi-two-level operation of multilevel inverters can be implemented using regular sampled SPWM, selective harmonic elimination or space vector modulation. However, space vector pulse-width modulation is considered in this paper for the reasons previously given. Quasi-two-level operation using space vector modulation can be realised by two different methods. The first method ignores the internal triangular regions within each sector of the space vector diagram in Fig. 3. Instead each sector of space vector diagram is treated as one triangular region. The switch states on the circumference of the main triangular region are used regardless of the voltage vector location within each sector. Thus, the switching sequence when the voltage vector is located in the first sector will be



$000 \rightarrow 100 \rightarrow 200 \rightarrow 300 \rightarrow 400 \rightarrow 410 \rightarrow 420$
$430 \rightarrow 440 \rightarrow 441 \rightarrow 442 \rightarrow 443 \rightarrow 444//444 \rightarrow$
$443 \rightarrow 442 \rightarrow 441 \rightarrow 440 \rightarrow 430 \rightarrow 420 \rightarrow$
$410 \rightarrow 400 \rightarrow 300 \rightarrow 200 \rightarrow 100 \rightarrow 000$

The average currents drawn from the intermediate dc link nodes 1 –3 with the first method in the first sector can be expressed as follows

$$\begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} = \begin{bmatrix} d_{100} & d_{410} & d_{420} \\ d_{200} & d_{420} & d_{442} \\ d_{300} & d_{430} & d_{443} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

Since the dwell time at nodes 1–3 are set the same, Td , within each switching cycle, the average currents drawn from these nodes must be zero according to i1 = i2 = i3 = d(i_a + i_b + i_c) = 0, where d ¼ (T_d/T_s). Theoretically, this means the dc link of a five-level inverter when operated in quasi-two level will remain balanced, as with a standard three- level inverter (assumes perfect modular without errors in calculations of switching instants over full fundament period, ignoring non-linearity of the switching devices, and equal dc link capacitors). Practically, a capacitor voltage-balancing strategy is needed to ensure correct voltage sharing between the dc link capacitors under all practical cases, such as transient conditions, load imbalance and imperfect modulators.

The second space vector modulation (SVM) method considers each sector of the space vector diagram to be comprised of many layers. For example, in a five-level inverter case, Fig. 3, the first sector comprises four layers A, B, C and D. Therefore the switch sequence is determined based on the location of the target voltage vector within the sector. For example, if the target voltage vector is located in layer D, the resultant switching sequence is the same as the first method. If the voltage vector is located in layer C, there two possible switching sequences:

(1) $000 \rightarrow 100 \rightarrow 200 \rightarrow 300 \rightarrow 310 \rightarrow 320 \rightarrow 330 \rightarrow 331 \rightarrow 332 \rightarrow 333//333 \rightarrow 332 \rightarrow 331 \rightarrow 330 \rightarrow 320 \rightarrow 310 \rightarrow 300 \rightarrow 200 \rightarrow 100 \rightarrow 000.$
(2) $111 \rightarrow 211 \rightarrow 211 \rightarrow 311 \rightarrow 411 \rightarrow 421 \rightarrow 431 \rightarrow 441 \rightarrow 442 \rightarrow 443 \rightarrow 444//444 \rightarrow 443 \rightarrow 442 \rightarrow 441 \rightarrow 431 \rightarrow 321 \rightarrow 411 \rightarrow .311 \rightarrow 211 \rightarrow 111.$

If the reference voltage vector is located in layer B, three possible switching sequences can be formed,

in similar way as for layer B, but requires fewer switch states. Therefore the second method may produce lower switching losses at medium and lower modulation indices as a result of a considerable reduction in the number of switching transitions required per switching cycle. The average currents drawn from the dc link nodes 1 – 3, with the sequence (i), can be expressed as

$$\begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} = \begin{bmatrix} d_{100} & d_{310} & d_{331} \\ d_{200} & d_{320} & d_{332} \\ [d_{300}+d_{310}+d_{320}] & 0 & -[d_{330}+d_{331}+d_{332}] \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 3\delta[i_a - i_c] \end{bmatrix} \quad (2)$$

Since non-zero current is drawn from node 3 with this switching sequence, capacitor i3 will be charged or discharged depending on the relative direction of i3.

Similarly, the average currents drawn from dc link nodes 1 – 3 with sequence (ii), when the reference voltage vector is located in the third layer, can be expressed as

$$\begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} = \begin{bmatrix} -[d_{211}+d_{311}+d_{411}] & 0 & [d_{421}+d_{431}+d_{441}] \\ d_{211} & d_{421} & d_{442} \\ d_{311} & d_{431} & d_{443} \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -3\delta[i_a - i_c] \\ 0 \\ 0 \end{bmatrix} \quad (3)$$

When sequence (ii) is used, non-zero current is drawn from node 1; as a result, the capacitor C1 will be charged or discharged depending on direction of i_1. Equations (1) –(3) show the first method always draws zero net currents from dc link nodes 1 – 3. As a result, the first method is expected to perform better than the second method in terms of dc link capacitor voltage balancing. Based on the balancing grounds, the first method is favoured over the second method in avoiding severe dc link capacitor voltage imbalance problems.

Since the switch states on the circumference of each sector are normally utilized, calculation of dwell times T1 , T2 and T0 corresponding to the main voltage vectors V1 , V2 and V0 based on two-level space modulation. Therefore T1, T2 and T0 are given by

$$\begin{aligned} T_1 &= m_a T_s \sin\left(\frac{\pi}{3} - \theta\right) \\ T_2 &= m_a T_s \sin\theta \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \quad (4)$$

Where ma = $2/\sqrt{3}$ (V_{ref} /V_{dc}) is the modulation index.

In order to establish the theoretical maximum modulation index limit for space vector-based quasi-two-level operation of a five-level inverter, consider the first sector of the space vector diagram in Fig. 3. In this sector, the maximum duty cycle, based on two-level space vector modulation, is

$$D = \frac{1}{T_s}[T_1 + T_2 + \frac{1}{2}T_0] = \frac{1}{2}\left[1 + \frac{T_1}{T_s} + \frac{T_2}{T_s}\right] \quad (5)$$

Substituting (4) into (5), the following expression for duty cycle is obtained

$$D = \frac{1}{2}\left[1 + m_a \sin\left(\theta + \frac{\pi}{3}\right)\right] \quad (6)$$

For fixed dwell times, the condition for maximum modulation index, before over-modulation, can be obtained, without creating voltage imbalance at the dc link. This condition is developed when a restriction on maximum allowable pulse width is imposed to prevent pulse dropping and switching of more than one voltage levels at any instant (as a result of no time left from the switching cycle to implement the dwell times in order to achieve smooth transition during the switching).

$$\frac{1}{2}\left[1 + m_a \sin\left(\theta + \frac{\pi}{3}\right)\right] \le 1 - 3\delta \quad (7)$$

The maximum pulse width is attained when θ+ (π/3) = π/2, therefore the maximum attainable modulation index is ma<= 1-6 δ. This limit is the same as that achieved with SPWM, as demonstrated in [16]. However, the dc link utilisation with space vector modulation is better than with SPWM for the same modulation index, which results in higher output voltage than SPWM, by a factor of (2/ 3) (which is 15.5% extra).

IV. REVIEW OF DWELL TIME BALANCING STRATEGY

The balancing strategy maintains voltage sharing between the dc link capacitors by adjusting the voltage output dwell time at nodes 1–3 [16]-[21]. The node dwell times are decided based on the direction of the currents at each node and the voltage deviation direction of each dc link capacitor from its reference voltage (1/(N 2 1))Vdc [16]. The voltage deviation of each dc link capacitor is defined as ΔVci = (1/(N-1))Vdc – Vci, and i = {1,2,……,N-1}, that is, ΔVci = (1/4)Vdc – Vci for a five level inverter. Assuming the current directions in Fig.1 as positive and the maximum and minimum dwell times at each node are $\hat{T}$ and $\check{T}$ the dwelling time capacitor voltage balancing strategy is summarized as [16].

1. $\Delta V_{ci} \times I_i < 0$, set $T_d = \hat{T}$.
2. $\Delta V_{ci} \times I_i > 0$, set $T_d = \check{T}$.

For more details on the dwell time control-balancing Strategy, refer to [16]-[21].

V. THREE-LEVEL OPERATION OF A DIODE-CLAMPED MULTILEVEL INVERTER

In an attempt to improve output voltage waveform quality and reduce switching losses, three-level operation of diode-clamped multilevel inverter is investigated as a potential alternative to quasi-two-level operation of diode-clamped inverters. In a three-level operation mode, the five-level diode-clamped inverter in Fig. 1 is operated as a three-level inverter, with the switching technique modified to prevent switching of more than one voltage level during the transition between 21/2Vdc to 0 and 0 to +1/2Vdc through 21/4Vdc and +1/4Vdc , respectively (see Fig. 4a).

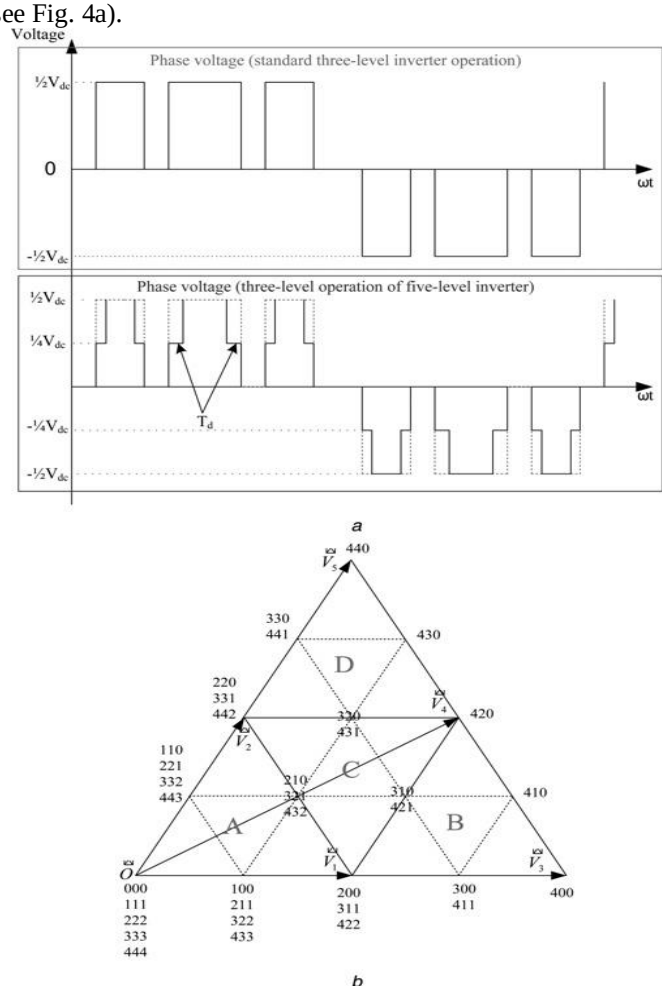


Fig.4. Phase voltage and space vector diagram for three-level operation of a five – level diode-clamped inverter.

a. Expanded version of phase voltage referred to node 2
b. First sector of space vector diagram of a five-level inverter

The modification introduced in the switching technique permits smooth transition between the dc link nodes 0 (voltage level -1/2Vdc) to 2 (voltage level 0) through node 1 (voltage level -1/4Vdc) and between nodes 2 –4 (voltage level +1/2Vdc) through node 3 (voltage level + 1/4Vdc). The maximum dwell time at nodes 1 and 3 is Td , which can be adjusted in order to maintain the voltage balance of dc link capacitors, taking into consideration the current direction at nodes 1 and 3. Node 2 is maintained at 1/2Vdc with respect to both the positive and negative dc rail using standard line-to-line voltage redundancy of the three-level diode-clamped inverter. Fig. 4b shows the five-level inverter space vector diagram used to achieve three-level operation of the diode- clamped inverter in Fig. 1. Labels A, B, C and D depicted the regions in the first sector of the five-level space vector diagram. The switching sequence is selected according to the target vector location to besynthesised. For example, if the target vector is located in region B, the only possible switching sequence using symmetrical modulation (three nearest vectors plus one redundant vector) is: 200 → 300 → 400 → 410 → 420 → 421 → 422/422 → 421 → 420 → 410 → 400 → 300 → 200. With this switching sequence, the average currents drawn from the dc link nodes 1–3 within each switching period are

$$\begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} = \begin{bmatrix} 0 & d_{410} & d_{421} \\ d_{200} - d_{422} & d_{420} + d_{421} & 0 \\ d_{300} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (8)$$

Where i^1 , i^2 and i^3 are the average currents drawn from the intermediate nodes of the dc link 1 – 3 with in one switching period, d410 = d421 = d300 = δ, and d200 + d422 = (T1/Ts). T_1 represents the time shared between the two redundant switch states (200 and 422) that represent voltage vector V1 so as to maintain the potential of the node 2 at 1/2Vdc with respect to the positive and negative rails. When the target vector is located at region C, the two possible switching sequences using symmetrical modulation are

a). 200 → 210 → 220 → 320 → 420 → 421 → 422//422 → 421 → 420 → 320 → 220 → 210 → 200.

b). 220 → 320 → 420 → 421 → 432 → 442// 422 → 432 → 422 → 421 → 420 → 320 → 220.

The average currents drawn from nodes 1 – 3 within each switching period when the target vector is located in region C and switching sequences (a) and (b) are applied are expressed by (9) and (10)

$$\begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} = \begin{bmatrix} 0 & d_{210} & d_{421} \\ d_{220} + d_{210} - d_{422} & d_{420} + d_{421} + d_{d320} & -d_{220} \\ d_{320} & 0 & 0 \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & d_{421} \\ -d_{422} & d_{420} + d_{421} + d_{320} & d_{442} - d_{220} + d_{432} \\ d_{320} & d_{432} & 0 \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (10)$$

Equation (8) shows that the dc link capacitor voltages can be maintained at 1/4Vdc independent of load power factor only if δ=0, and the redundant switch states corresponding to vector V1 (with duty cycles d200 and d422) are utilised to maintain zero mean current from dc link nodes 1 –3. A similar problem exists when the target located in region C, with both switching sequences (a) and (b). For this reason, the dc link capacitor

voltage balancing of the diode-clamped inverter when operated in a three-level mode remains power factor-dependent. The times T0 through T5, corresponding to voltage vectors V0 through V5 , are calculated using standard three-level space vector modulation, then the dwell time Td is introduced at states, such as (300, 411), 410 and (310, 421), to allow smooth transition between 200– 400, 400– 420 and 420– 422 without switching of two voltage levels. As a result, low
Dv/dt and low switching losses are possible owing to a significant reduction in a number of switch states required per switching period. In general, it can be noticed that three-level operation of diode-clamped multilevel inverters is only possible when number of levels is odd.

VI. PERFORMANCE EVALUATION OF THREE- LEVEL OPERATION

Fig. 5 shows the results obtained when a five-level diode - clamped inverter is operated in a three-level mode with a modulation index of 0.9, feeding a three-phase static load with 0.8 power factor lagging. Three-level operation of the five-level diode-clamped inverter is implemented using space vector modulation as explained above, with a switching frequency of 2.1 kHz and dc link capacitance of 2.2 mF. Figs. 5a– c show the line voltage, load current and dc link capacitor voltages. It is observed that three -level operation of the diode-clamped inverter produces voltage and current waveforms with limited distortion, and the dc link capacitor voltages are not equally distributed across the four dc link capacitors as shown in Fig.5c. This is because the mean currents from the dc link nodes 1 and 3 cannot be forced to zero for non-zero values of dwell time as demonstrated by (8) – (10). This increases the voltage stress across some of the circuit devices. This voltage imbalance increases when the power factor approach unity. Fig. 6 shows the results obtained when a five-level inverter is operated in three-level mode with 0.8 modulation index and 0.67 power factor lagging. These results show that the quality of current waveforms is improved and distribution of the dc voltage across the four dc link capacitors voltages is better compared to that in Fig. 5c. This demonstrates that the capacitor voltage balancing of the diode-clamped inverter operated in three-level mode is power factor - dependent as in standard multilevel operation of diode-clamped inverter with more than three levels. The only difference is that the mean currents drawn from the nodes 1 and 2 are smaller than that with full multilevel operation. The lower averages node currents result in relatively smaller voltage drift from the desire set point. However, the voltage drift from 1/4Vdc is worse at unity power factor. Also it can be noticed that the dc link capacitors voltage ripple with three-level operation is large despite the use of relatively large capacitance compare to that use for quasi-two-level operation.

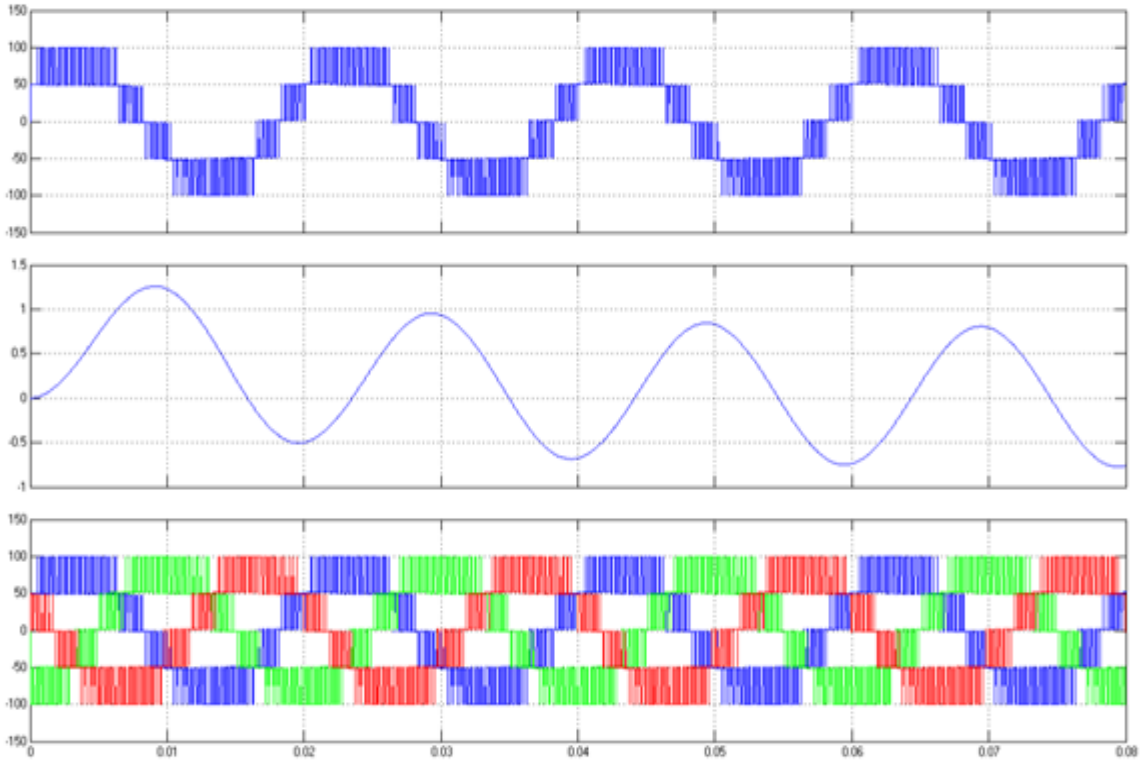


Fig (a) Output voltage, current and three phase wave forms of Quasi 3 level inverter using SPWM

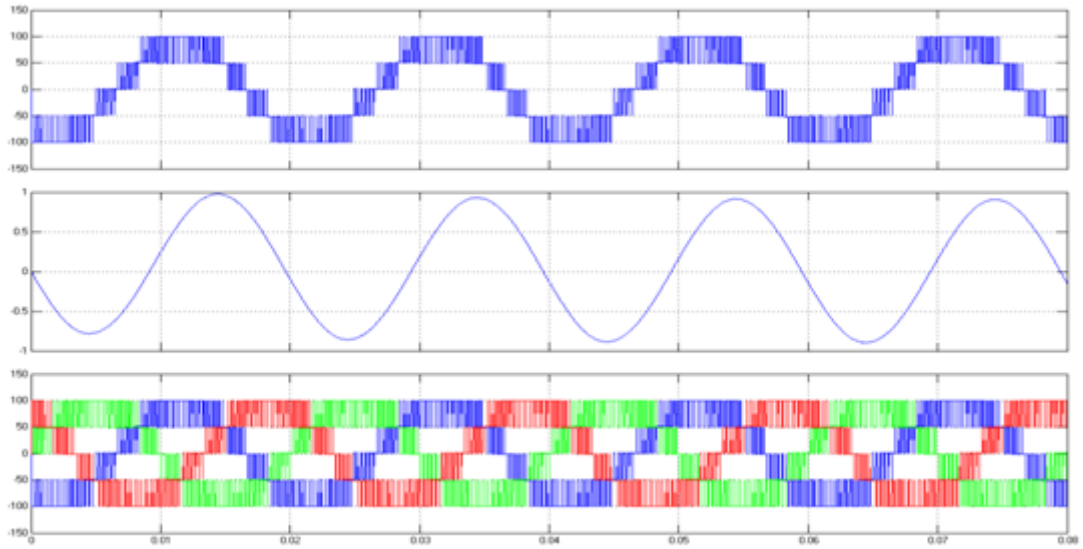


Fig (b) Output voltage, current and three phase wave forms of Quasi 3 level inverter using SVM

Fig. 5 Voltage and current waveforms demonstrating the concept of three-level operation of a diode-clamped inverter (dc link voltage is 200 V, switching frequency 2.1 kHz, modulation index, M = 0.9 and load power factor is 0.8 lagging)

a) Line voltage (total harmonic distortion (THD) = 29.78%). Scale (x-axis: 5 ms/div and y-axis: 100 V/div)

b) Three-phase load currents. Scale (x-axis: 2.5 ms/div and y-axis: 2 A/div)

c) Voltage across the four link capacitors. Scale (x-axis: 50 ms/div and y-axis: 20 V/div)

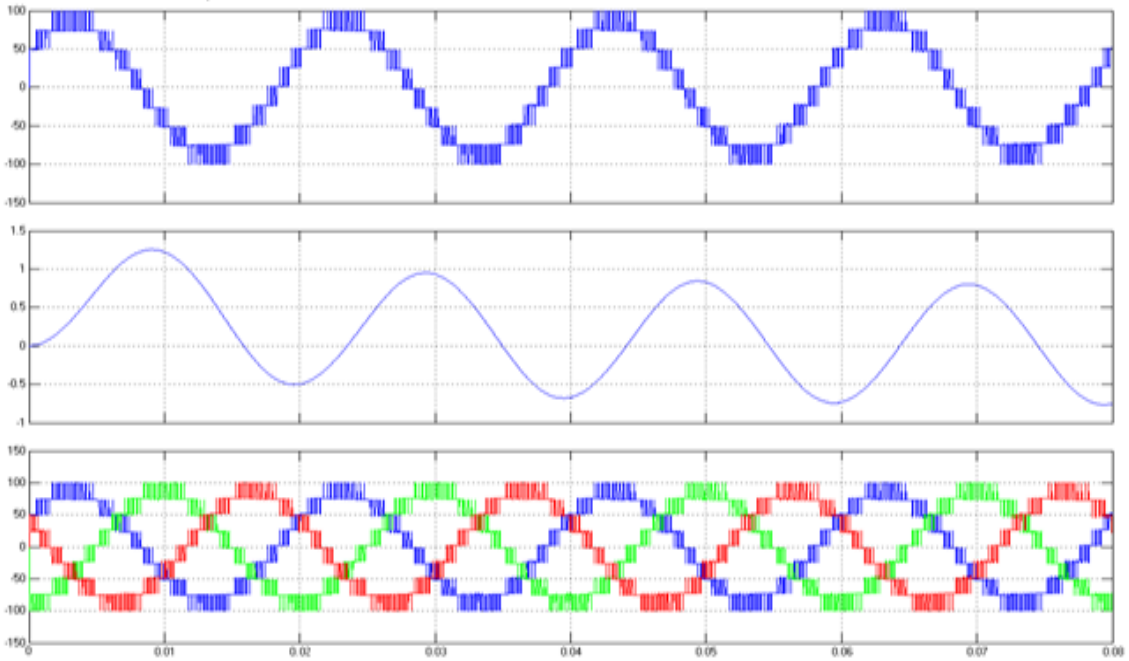


Fig (a) Output voltage, current and three phase waveforms for SPWM operation of 5-level inverter voltage

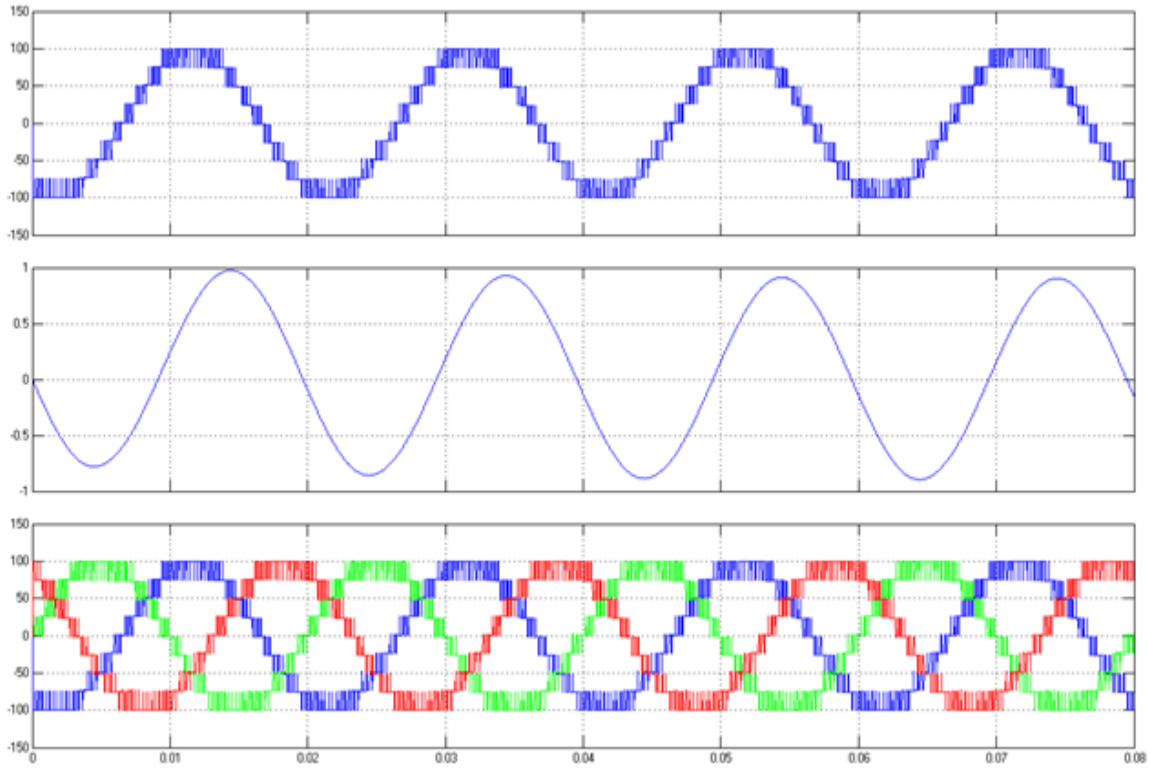


Fig (b) Output voltage, current and three phase wave forms of five level inverter using SVM

Fig. 6 Voltage and current waveforms obtained when a three-phase five-level diode-clamped inverter is operated in three-level mode with 200 V dc link, modulation index ¼ 0.8 and power factor ¼ 0.67 lagging)

a) Line voltage. Scale (x-axis: 5 ms/div and y-axis: 100 V/div)

b) Three-phase load currents. Scale (x-axis: 2.5 ms/div and y-axis: 2 A/div)

c) Voltage across the four dc link capacitors. Scale (x-axis: 100 ms/div and y-axis: 10 V/div)

VII. CONCLUSIONS

This paper investigates the use of space vector modulation - based quasi-two-level operation of diode-clamped inverter to maximise dc link utilisation, reduce dc link capacitance, avoid dc link capacitor voltage imbalance and improve the quality of output voltage by placing the dominant harmonic components beyond and around second switching frequency components. This approach produces an inverter viable for medium-voltage applications where a large amount of active power exchange is required, such as drive systems and grid - connected inverters for integration of renewable energy resources. In attempt to improve output voltage waveform quality and reduce switching loss, this paper investigated the extension of quasi-two-level operation concept of the diode - clamped multilevel inverter to three-level operation. It is established that three-level operation requires large dc link capacitance and dc link capacitor voltage balancing is power factor- and dwell time-dependent.

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AUTHORS

K. Rajesh born in Tirupathi. He is completed his B.Tech in 2010 from SITE, Puttur Affiliated to JNTUA. He is currently perusing M.Tech in SVPCET, Puttur. His areas of interest is Power electronic converters, Facts devices.

K.Vijaya Bhaskar born in Puttur. He is completed his B.tech in 2007 from JNTUA. He is completed M.Tech in 2010 from JNTUA. His area of interest is Neural networks & Fuzzy systems, Application in Power systems.