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New Efficient Bridgeless Cuk Rectifiers for PFC Application on d.c machine

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Abstract:- Three new bridgeless single-phase ac–dc power factor correction (PFC) rectifiers based on Cuk topology are proposed. The proposed topologies are designed to work in discontinuous conduction mode (DCM) to achieve almost a unity power factor and low total harmonic distortion of the Input current. The DCM operation gives additional advantages such as zero-current turn-ON in the power switches, zero-current turn-OFF in the output diode, and simple control circuitry. proposed topology is worked on discrete d.c machine .To show the performance between resistance load and discrete d.c machine.

Index Terms:- Bridgeless rectifier, Cuk converter, low conduction losses, power factor correction (PFC), rectifier, single-ended primary-inductor converter (SEPIC) converter, total harmonic distortion (THD).

I. INTRODUCTION

POWER supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards, such as the IEC 61000-3-2. Most of the PFC rectifiers utilize a boost converter at their front end. In an effort to maximize the power supply efficiency, considerable research efforts have been directed toward designing bridgeless PFC circuits, where the number of semiconductors generating losses is reduced by essentially eliminating the full bridge input diode rectifier. A bridgeless PFC rectifier allows the current to flow through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced and higher efficiency can be obtained, as well as cost savings. Recently, several bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduce noise emissions via soft-switching techniques or coupled magnetic topologies [1]–[9]. the voltage. To overcome these drawbacks, several bridgeless topologies, which are suitable for step-up/step-down applications have been recently introduced in [10]–[13]. However, the proposed topology in [10] still suffers from having three semiconductors in the current conduction path during each switching cycle. In [11]–[23], a bridgeless PFC rectifier based on the single ended primary-inductance converter (SEPIC) topology is presented. Similar to the boost converter, the SEPIC converter has the disadvantage of discontinuous output current resulting in a relatively high output ripple. However, the input line current cannot follow the input voltage around the zero crossings of the input line voltage; besides, the output to input voltage ratio is limited to half. Also, buck PFC converter results in an increased total harmonic distortion (THD) and a reduced power factor [15]. The Cuk converter offers several advantages in PFC applications, such as easy implementation of transformer isolation, natural protection against inrush current occurring at start-up or

Overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the discontinuous conduction mode (DCM) topology [16], [17]. Unlike the SEPIC converter, the Cuk converter has both continuous input and output currents with a low current ripple. Thus, for applications, which require a low current ripple at the input and output ports of the converter, the Cuk converter seems to be a potential candidate in the basic converter topologies

II. PROPOSED BRIDGELESS CUK PFC RECTIFIERS

The three proposed bridgeless Cuk PFC rectifiers are shown in Fig.1. The proposed topologies are formed by connecting two dc–dc Cuk converters, one for each half-line period ($T/2$) of the input voltage. It should be mentioned here that the topology of Fig. 1(a) was listed in [12] as a new converter topology but not analyzed. The operational circuits during the positive and negative half-line period for the proposed bridgeless Cuk rectifiers of Fig. 1(a)–(c) are shown in Figs. 2–3, respectively. Note that by referring to Figs. 2–3, there are one or two semiconductor(s) in the current flowing path; hence, the current stresses in the active and passive switches are further reduced and the circuit efficiency is improved compared to the

conventional Cuk rectifier. In addition, Fig. 1(a) and (c) shows that one rail of the output voltage bus is always connected to the input ac line through the slow-recovery diodes *Dp* and *Dn* or directly as in the case of the topology of Fig. 1(b). Thus, the proposed topologies do not suffer from the high common-mode EMI noise emission problem and have common-mode EMI performance similar to the conventional PFC topologies. Consequently, the proposed topologies appear to be promising candidates for commercial PFC products.

The proposed bridgeless rectifiers of Fig. 2 utilize two power switches (*Q*1 and *Q*2). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Compared to the conventional Cuk topology, the structure of the proposed topologies utilizes one additional inductor,

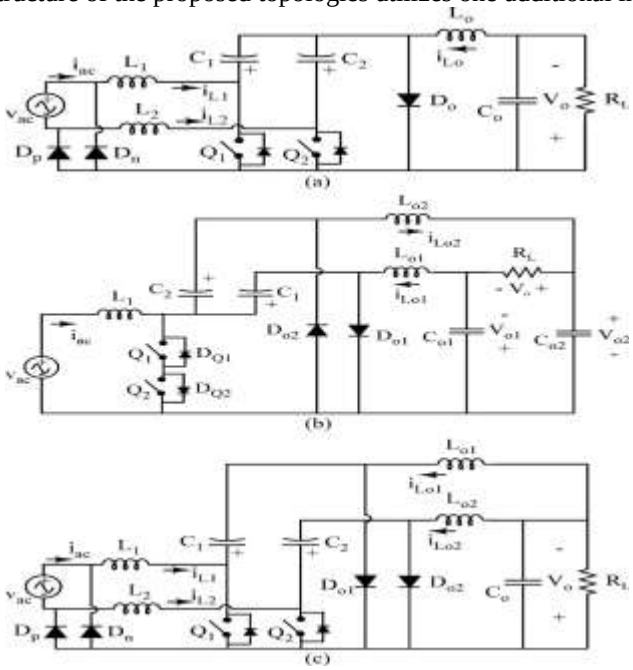

Fig.1. Proposed bridgeless Cuk PFC rectifiers. (a) Type 1. (b) Type 2. (c) Type 3.

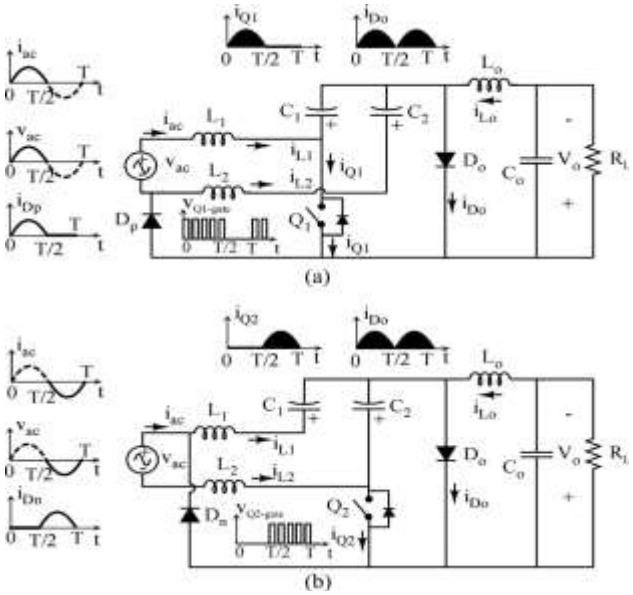

Fig. 2. Equivalent circuits for the type-1 rectifier. (a) During positive half-line period. (b) During negative half-line period of the input voltage.

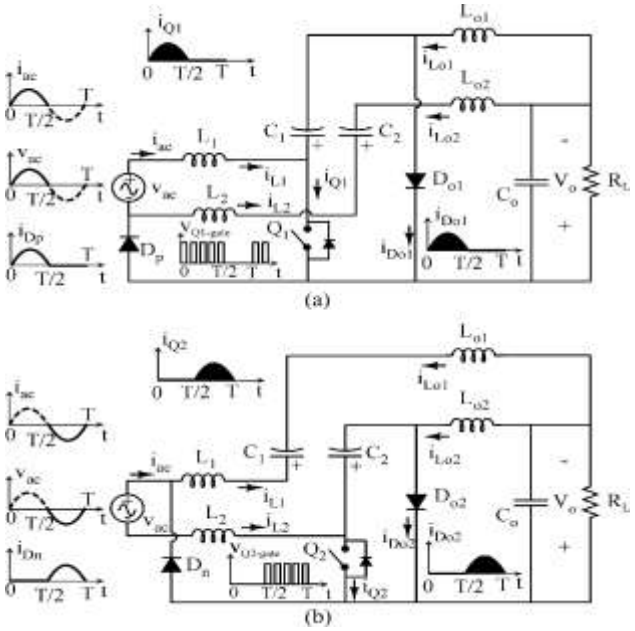

Fig. 3. Equivalent circuits for type-3 rectifier. (a) During positive half-line period. (b) During negative half-line period of the input voltage.

This is often described as a disadvantage in terms of size and cost. However, a better thermal performance can be achieved with the two inductors compared to a single inductor. It should be mentioned here that the three inductors in the proposed topologies can be coupled on the same magnetic core allowing considerable size and cost reduction. Additionally, the "near zero-ripple-current" condition at the input or output port of the rectifier can be achieved without compromising performance

III. PRINCIPLE OF OPERATION

The proposed bridgeless type-1 Cuk rectifier of Fig. 1(a) will be considered in this study. Type 1 is similar to type 3, except for the output stage stresses. The SEPIC version of type 2 has been analyzed in [19]. The analysis assumes that the converter is operating at a steady state in addition to the following assumptions: pure sinusoidal input voltage, ideal lossless components, and all capacitors are large enough such that their switching voltage ripples are negligible during the switching period *Ts* .Moreover, the output filter capacitor *Co* (*Co* 1 and *Co* 2 for topology 2) has a large capacitance such that the voltage across it is constant over the entire line period. Referring to Fig. 2(a), during the positive half-line cycle, the first dc–dc Cuk circuit, *L*1–*Q*1–*C*1–*Lo* 1–*Do* , is active through diode *Dp* , which connects the input ac sourceto the output. During the negative half-line cycle, as shown in Fig. 2(b), the second dc–dc Cuk circuit, *L*2–*Q*2 -*C*2–*Lo* 2–*Do*, is active through diode *Dn* , which connects the input ac source to the output. As a result, the average voltage across capacitor *C*1during the line cycle can be expressed as follows:

$$v_{C_1}(t) = \begin{cases} v_{ac}(t) + V_o, & 0 \le t \le \dfrac{T}{2} \\ V_o, & \dfrac{T}{2} \le t \le T \end{cases}. \qquad (1)$$

Due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half cycle of the input voltage. Moreover, the operation of the proposed rectifiers of Fig. 1 will be described assuming that the three inductors are operating in DCM. By operating the rectifier in DCM, several advantages can be gained. These advantages include natural near-unity power factor, the power switches are turned ON at zero current, and the output diode (*Do*) is turned OFF at zero current. Thus, the losses due to the turn-ON switching and the reverse recovery of the output diodes are considerably reduced. Conversely, DCM operation significantly increases the conduction losses due to the increased current stress through circuit components. As a result, this leads to one disadvantage of the DCM operation, which limits its use to low-power applications (<300 W) [18].Similar to the conventional Cuk converter, the circuit operation in DCM can be divided into three

distinct operating stages during one switching period *Ts*. Equivalent circuits over a switching period *Ts* in the positive half-line period of Fig. 2(a) The topological stages of type 1 over a switching cycle can be briefly described as follows.

*Stage 1[t*0, *t*1 *], :* This stage starts when the switch *Q*1 is turned ON. Diode *Dp* is forward biased by the inductor current *iL*1. As a result, the diode *Dn* is reverse biased by the input voltage. The output diode *Do* is reverse biased by the reverse voltage (*v*ac + *Vo*), while *Do* is reverse biased by the output voltage *Vo* . In this stage, the currents through inductors *L*1 and *Lo* 1 increase linearly with the input voltage, while the current through *Lo* 2 is zero due to the constant voltage across *C*2. The inductor currents of *L*1 and *Lo* 1 during this stage are given by

$$\frac{di_{Ln}}{dt} = \frac{v_{ac}}{L_n}, \qquad n = 1,\ o1. \tag{2}$$

Accordingly, the peak current through the active switch *Q*1 is given by

$$I_{Q1,\mathrm{pk}} = \frac{V_m}{L_e} D_1 T_S \tag{3}$$

Where Vm is the peak amplitude of the input voltage *v* ac, *D*1 is the switch duty cycle, and *Le* is the parallel combination of inductors *L*1 and *Lo* 1 .

*Stage 2[t*1, *t2]:* This stage starts when the switch *Q*1 is turned OFF and the diode *Do* 1 is turned ON simultaneously providing a path for the inductor currents *iL* 1 and *I Lo*1 . The diode *Dp* remains conducting to provide a path for *iL* 1 . Diode *Do* remains reverse biased during this interval. This interval ends when *iDo* reaches zero and *Do* 1 becomes reverse biased. Note that the diode *Do* is switched OFF at zero current. Similarly, the inductor currents of *L*1 and *Lo* 1 during this stage can be represented as follows:

$$I_{Q1,\mathrm{pk}} = \frac{V_m}{L_e} D_1 T_S \tag{3}$$

$$\frac{di_{Ln}}{dt} = -\frac{V_o}{L_n}, \qquad n = 1,\ o1. \tag{4}$$

*Stage 3[t*2, *t*3 *]:* During this interval, only the diode *Dp* conducts to provide a path for *iL* 1 . Accordingly, the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor *C*1 is being charged by the inductor current *iL* 1 . This period ends when *Q*1 is turned ON. By applying inductor volt-second across *L*1 and *Lo* 1 , the normalized length of the second stage period can be expressed as follows:

$$D_2 = \frac{D_1}{M} \sin \omega t \tag{5}$$

where ω is the line angular frequency, and *M* is the voltage conversion ratio (*M* = *Vo* /*Vm*). Since the diode *Dp* continuously conducts throughout the entire switching period, the average voltage across *C*2 is equal to the output voltage *Vo* . As a result, a negligible ac current will flow through *C*2 and *Lo* 2 . Therefore, the current through *L*2 during the positive half cycle of the input voltage is equal to the negative current through the body diode of *Q*2 . It should be noted that the body diode of the inactive switch *Q*2 is always conducting current during the positive half cycle of the input voltage. This is due to the low impedance of the input inductors (*L*1 and *L*2) at the line frequency. Therefore, the input diode *Dp* and body diode of *Q*2 appear in parallel configuration to share the return current. A large portion of the return current will pass through the diode that has a lower voltage drop. The efficiency of the converter can be slightly improved by using synchronous rectification to turn ON the switch *Q*2 during the positive half cycle of the input voltage, which eliminates its body-diode conduction.

IV. MATLAB MODELING AND SIMULATION RESULTS

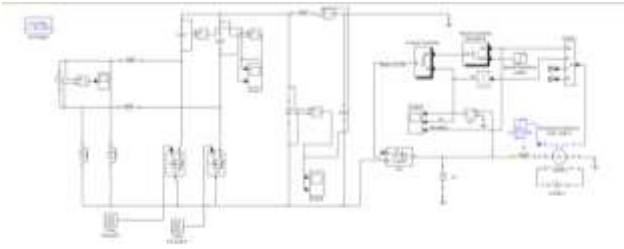

Fig.4 Matlab/Simulink Model of Proposed efficient bridgeless rectifier with d.c machine

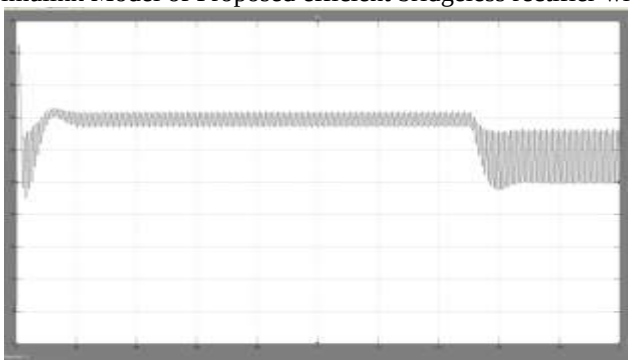

Fig.5 Output Voltage

Fig.6 Output Current

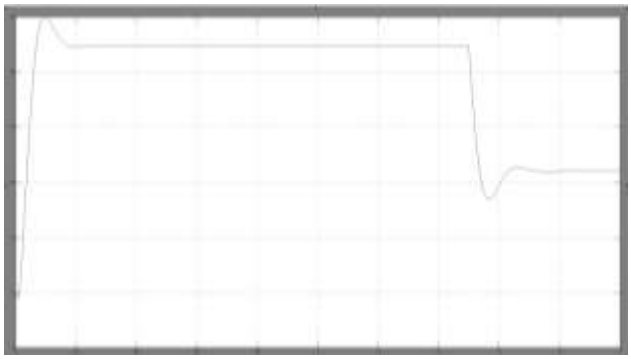

Fig.7 Output speed

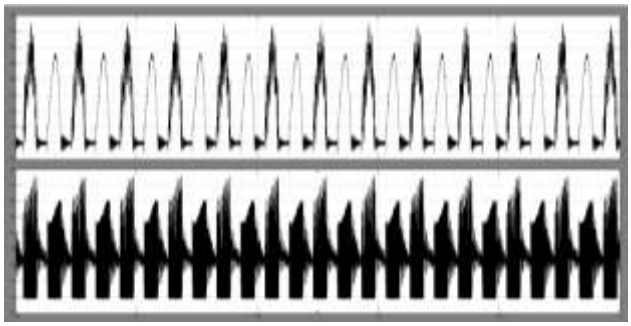

Fig 8 voltage of inductor l1&l2

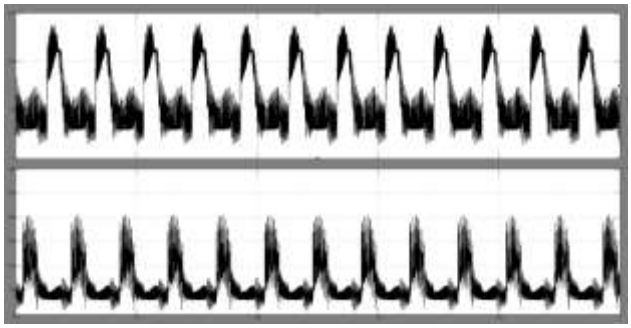

Fig 9 voltage & current of inductor 3

V. CONCLUSION

Three single-phase ac–dc bridgeless rectifiers based on Cuk topology are presented and discussed in this paper. The validity and performance of the proposed topologies are verified by simulation and experimental results. Due to the lower conduction and switching losses, the proposed topologies can further improve the conversion efficiency when compared with the conventional Cuk PFC rectifier. Namely, to maintain the same efficiency, the proposed circuits can operate with a higher switching frequency. Thus, additional reduction in the size of the PFC inductor and EMI filter could be achieved. The proposed bridgeless topologies can improve the efficiency by approximately 1.4% compared to the conventional PFC Cuk rectifier. The performance of two types of the proposed topologies was verified on a 150Wexperimental prototype. The measured efficiency of the prototype rectifier at 100 Vrms line and full load is above 93% with THD below 2%. Experimental results are observed to be in good agreement with simulation results.

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